OPTOELECTRONIC PROPERTIES OF GRAPHENE/OXIDE/SEMICONDUCTOR STRUCTURE WITH NANO-CHANNELS

by

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Metal-oxide-semiconductor (MOS) structure is a basic building block of silicon CMOS electronics. The silicon surface, when passivated by thermally grown oxide, can harbor a good quality two-dimensional electronic system (2DES). We have developed a graphene/oxide/nano-channel-etched Si (GOS) capacitor structure and investigated the photodetection properties. In this structure photogenerated carriers are extracted through a thin oxide layer via tunneling process and a monolayer graphene is used as a transparent conducting electrode. Nano-channels of high aspect ratio (length to diameter ratio of ~100 with diameter < 100nm) are formed in Si using a non-lithographic electrochemical process, metal-assisted-chemical-etching (MACE). We introduced a thin oxide layer in the MACE process for controlled formation of nano-channels. The nano-channel-etched Si demonstrates an antireflection effect. The current-versus-voltage (I-V) characteristic of GOS structure is measured both in dark and under illumination at 633 nm wavelength. Tunneling of carriers through the thin (2-4nm) oxide layer as well as ballistic transport through nano-channels is discussed as underlying mechanisms of carrier transport. A photo responsivity of 0.33 A/W and internal quantum efficiency of 84 % is observed on graphene/SiO_2/nano-channeled n-Si structure.

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1.0 INTRODUCTION

1.1 GRAPHENE

Graphene is a monolayer of carbon atoms densely packed in hexagonal lattice structure. Graphene has special electrical, optical and magnetic properties, such as high carrier mobility up to ~15000 $cm^2 (Vs)^{-1}$ at room temperature [1], quantum Hall effect under room temperature, excellent absorption of white light which make it transparent, high scalability and so forth. Recently researchers have developed various ways to produce single layer graphene with high quality, for example, mechanical and chemical exfoliation, chemical vapor deposition (CVD) on transient metal surface, and reduction of single-layer graphene oxide [2].

Carbon nanotubes (CNTs) have been studied for over 30 years and single-walled nanotubes share many common properties with graphene. Graphene had already been discussed theoretically long time ago starting at 1947 by P.R. Wallace [3], later the wave equation for excitations, the similarity to the Dirac equation. But not after when the possibility of producing monolayer graphene was proved by Novoselov et al., demonstrating that a single layer of carbon could be peeled off and transferred from graphite which consists of many stacked hexagonal carbon sheets in 2004, did people started to turn to graphene from CNT. Research related to graphene and its special properties has suddenly exploded since 2005.

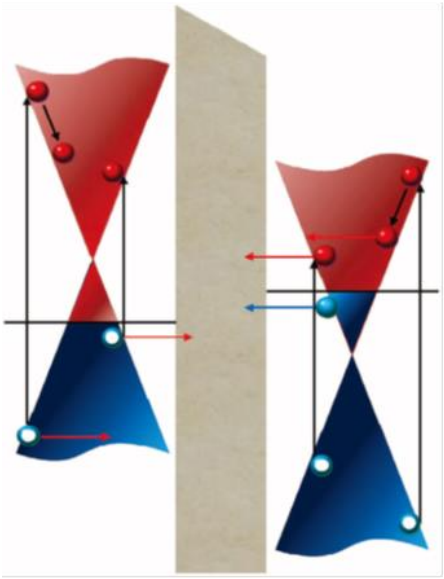
Undoped graphene is a semiconductor with zero bandgap. The resistivity of few-layer graphene varies little from 100 K to 300 K. However the conductivity will increase significantly as temperature goes up. Monolayer graphene has a higher resistivity than other few-layer

graphene. The Fermi level of the intrinsic graphene is located on the connection point (Dirac point) of conduction band and valence band. Therefore the undoped graphene has a relatively low thermal conductivity of 4.84×10^3 to 5.30×10^3 W/mK at room temperature due to the zero density of states at Dirac point [4]. However its Fermi level can be shifted up or down by applying external electric field, resulting in n-doped or p-doped graphene, respectively. Graphene can also be doped by adsorbing chemicals such as BV for n-type and $AuCl_3$ for p-type [5]. The doped graphene shows significantly higher electrical conductivity.

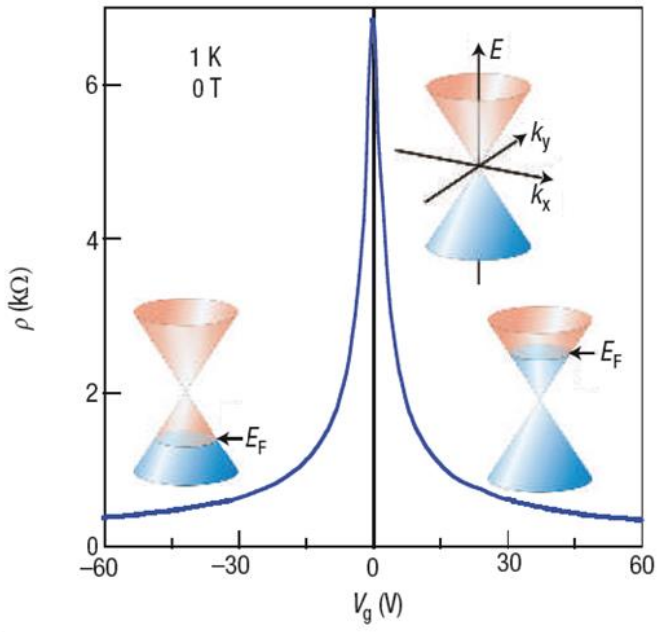
Graphene is a promising candidate for the new generation of conducting electrode materials because of its outstanding thermal, chemical and mechanical stability. Also, graphene is transparent over a broad spectral range, absorbing only 2.3% of incident light [6]. In this work we are interested in using graphene as a transparent conducting electrode for optoelectronic devices.

Xia et al. reported about ultrafast graphene photodetector up to 40 GHz using a laser of 1550 nm wavelength. No photoresponse degradation is observed and their calculation suggests that such graphene photodetectors may detect light with frequency over 500 GHz. More interestingly, the photo-generated carriers in the graphene photodetectors are transported intrinsically different from those in the semiconductor photodetectors [8]. Once incident light is absorbed, electron-hole pairs will be generated in graphene with recombination time less than 100 ps, which depends on the carrier concentration. The existence of external or internal field (built-in potential) will help the separation of electron-hole pairs and generate photocurrent. When no external voltage applied (open-circuit), only internal fields contribute to the separation. It produces an open-circuit voltage across the region while no photo current is generated. When the device is short-circuited, a photocurrent (short-circuit current) is produced. The carriers could

tunnel through the potential barrier of single-layer graphene easily, providing the possibility of high bandwidth photo detection under zero bias.



(a)



(b)

Figure 1 (a) Band diagram of graphene p–n diode under forward bias. Red bubbles represent electrons and white ones stand for holes. Arrows point out the moving directions of carriers which contribute to currents across the diode [5]. (b) Resistivity change and Fermi level shift of single-layer graphene under positive and negative bias. Positive V_g will introduce electrons which makes Fermi level move up close to conduction band, the graphene become n-type. Resistivity ρ decreases as the bias voltage goes high, indicating high mobility of "doped graphene" [7].

1.2 NANOSTRUCTURES IN ELECTRONICS

Silicon nanostructures such as silicon nanowire (SiNW) and silicon nano-channel have exhibited a promising potential of applications in various fields. For example, the power conversion efficiency of solar cell can be improved when silicon nanostructures are incorporated into the active or passivation layer. Dou et al. utilized silicon nanostructures made by metal-assisted-chemical-etching (MACE) on single crystal solar cell, achieving open circuit voltage of 0.565 V,, short circuit current of 0.15 A and maximum external quantum efficiency (EQE) of 70% under standard test condition. They reported the surface reflection reduced 5% in the 300 to1000 nm wavelength range [9]. Silicon nanostructures also have significantly lower thermal conductivity than bulk silicon, which makes the former a better material in thermoelectricity. Nanostructure with high aspect ratio and special carriers transport property can be used in sensor devices to get good accuracy and stability [10].

Vacuum, containing nothing that cause optical and acoustic phonon scattering, is a perfect medium for ballistic conduction which minimizes the power loss and quality degradation. Inside the vacuum tube, carriers will only collide with the wall when moving by field. Therefore electrical devices applying void channels (i.e., nanoscale vacuum channels) have the advantage of lower power supply requirement and higher operating frequency compared to traditional solid-state semiconductor devices.

Although carbon nanotubes and silicon nanowires could help achieve ballistic transport, it is difficult to integrate into traditional devices. However nano channels can be fabricated on

bulk silicon easily. Theoretically if the length of nano channel is greater than the mean free path for electrons in air, the channel can be considered as a vacuum channel even under atmospheric pressure. Dr. Kim's group demonstrated a metal–oxide–semiconductor (MOS) field-effect transistor with a vacuum channel with 20 nS/μm trans-conductance, 500 on/off current ratio and 0.5 V turn-on voltage in 2012 [11] [12]. Here the length of the vacuum channel is determined by the silicon oxide thickness of MOS and is designed to be smaller than the mean free path in air (~65nm).

2.0 FABRICATION

2.1 GRAPHENE/OXIDE/SEMINCONDUCTOR STRUCTURE

2.1.1 Wafer cleaning

We used (100) Si wafers (n-type or p-type doped) as substrate. The substrates were cleaned in solvent (trichloroethylene, acetone and methanol in ultrasonic bath for 5 min each) in order to remove organic contaminants. Subsequently, wafers were rinsed under running de-ionized (DI) water for 1 minute to remove remaining organic solvents. Finally wafers were blown dried by compressed nitrogen gas.

The RCA standard cleaning process is applied before thermal oxidation to assure the quality of silicon oxide grown on the Si substrate. For the first step of RCA standard cleaning (SC-1), a mixture of H_2O: H_2O_2 (30 wt%): NH_4OH (30 wt%) in 5:1:1 volume ratio is used to remove organic impurities and some metals. Si wafers are then immersed briefly in dilute hydrofluoric acid (49 wt % HF; diluted with DI water to 1/50 volume ratio) at room temperature in order to remove native oxide. For the next step (SC-2), a mixture of H_2O: H_2O_2 (30 wt %): HCl (38 wt %) in 6:1:1 volume ratio is used to remove remaining alkali and metals. Both solvents were heated to 70 – 80 ℃. Samples were cleaned in the hot bath solution for 10 minutes and then rinsed under running DI water for 1 minute. Cleaning was finished with nitrogen blow drying [13].

2.1.2 Thermal oxidation

A silicon dioxide layer with 40nm thickness was grown in dry air ambient at 950 ℃ for 72 min. For silicon dioxide thickness less than 10 nm, oxidation was performed at lower temperature: 832 ℃ for 5 minutes for 4 nm oxide and 2 minutes for 2 nm oxide. Use of lower temperature is for better control of grown oxide thickness. The thickness of 40 nm oxide was confirmed by stylus-based surface profiler (Alpha-step 200) scanning across trenches/steps created by photolithography and buffered-HF-solution etching. The thickness of ultra-thin oxide (~2nm) was confirmed by ellipsometer.

2.1.3 Self-organized silver nano-islands

A thin film of silver (~4 nm thickness) was deposited by thermal evaporation in the following steps. First, the samples were cut into approximately 2.5 cm x 2.5 cm pieces and mounted on a glass slide. Thermal evaporation deposition was started when the chamber pressure goes below 1.6 $x10^{-5}$ mTorr. Deposition rate was controlled to stay below 0.2 nm/s and was monitored by a quartz crystal thickness monitor. It is difficult to measure exact film thickness when it goes below 10 nm. Here the crystal monitor reading is used as a relative mass thickness, which we will refer to later. All deposition process was done at room temperature.

The deposited Ag film was anneal-treated in order to complete formation of self-organized silver nano-islands. Nitrogen gas was flown through the annealing tube at steady temperature of 250 ℃ for 30 min.

2.1.4 Metal-assisted chemical etching

A mixture of HF: H_2O_2: H_2O in 4:1:20 volume ratio is used as an etching solution. The etch rate of bare silicon dioxide is around 20 nm/min. The etchant barely attacks silicon with an etch rate below 1 nm/min. Samples with self-organized silver nano-islands were submerged into the etching solution with face up for 8 to 9 min, which results in etch depth of around 4 to 5 um.

The remaining silver on the surface was removed using strong acid solution: samples were immersed into a mixture of HNO_3 and HCl at 3 to 1 volume ratio for 4 minutes with agitation.

2.1.5 Chemical mechanical polishing (CMP)

Sample was mounted on a polishing sample holder with QuickStick 135 mounting wax melted at 160 ℃. 8 inch MultiTex polishing cloth was mounted onto Buehler Metaserv Grinder-Polisher for CMP. A weight was applied on the sample holder such that the pressure level is ~3000 N/m^2. Table 1 is a description of the process and abrasive suspension used on polishing cloth. Polishing direction was changed every 5 minutes for good uniformity. All the suspension materials were purchased from South Bay Technology. Total polishing time of 80 min resulted in removal of~1-μm-thickness of silicon.

9-micron Diamond Suspension: South Bay Tech Micro DI™ Permanent Diamond Suspension. It is a mixture of diamond and proprietary ingredients in a water base.

1-micron alumina abrasive suspension: South Bay Tech Aluminum Oxide Suspension De-agglomerated. It is a mixture of aluminum oxide, glycerine and proprietary suspending agents.

0.05-micron alumina abrasive suspension: South Bay Tech Aluminum Oxide Suspension De-agglomerated. It is a mixture of aluminum oxide, lubricants and surfactants.

Colloidal silica suspension (0.02 ~ 0.06 micron): South Bay Tech Colloidal Silica Suspension. It is a mixture of amorphous silica and water.

2.1.6 Silicon dioxide sputtering

The silicon dioxide films were deposited in an RF (13.56 MHz) magnetron sputtering system. The RF generator with impedance matching network had a maximum output power of 1500 W. A sputtering target was a 50.8 mm diameter and 3.175 mm thickness silicon dioxide piece of high purity (99.99%). The sputtering ambient was a gas mixture of 95% argon and 5% oxygen. The sputtering pressure was maintained at 20 mTorr and the RF power was 50W. The distance between the target and the substrate was 2.0 inch. The chamber base pressure was around 2×10^{-5} Torr. Before starting the deposition, a pre-sputtering was applied to remove any impurities on target and to stabilize sputtering power and pressure. Sputter deposition was performed at room temperature. However, the substrate temperature may rise because of plasma bombardment during deposition [14]. We deposited a 20 nm silicon dioxide layer with 1 nm/min deposition rate.

2.1.7 Metallization

The silicon dioxide on the bottom side of the sample was removed by BHF etching. Right after that, a 100-nm aluminum layer was deposited on the backside of the sample by thermal evaporation deposition. Deposition rate was around 1 nm/s. Annealing for Ohmic contact was carried out in nitrogen ambient at 350 ℃ for 30 min.

2.1.8 Graphene transfer

One common method of producing monolayer graphene is mechanical exfoliation. According to the paper published in 2004 by Novoselov et al., monolayer graphene can be peeled off using Scotch tape and then transferred to another substrate [1]. This method would provide good quality graphene but with low yield and smaller size flakes. In this work we have chosen CVD grown graphene as our source material and transferred to our substrates. CVD-grown monolayer graphene on 25-um-thick copper foil was purchased from Advanced Chemicals. Graphene on copper was cut into 1.5 mm x 1.5 mm square pieces. 2 um PMMA (4% in anisole) was spin coated on top of graphene with 3000 rpm spin rate for 1 min. These PMMA/graphene/Cu pieces were floated (with PMMA face up) on copper etchant for 30 min to remove backside copper. After that PMMA/graphene sheets were transferred to fresh DI water for 10 min to remove the etchant residue. The transfer cleaning process was repeated three times in DI water. Graphene with PMMA on top was subsequently transferred to our destination substrate. Then the sample was baked inside an oven at 70 ℃ for 2 h. Later the PMMA/graphene/substrate was immersed into acetone and methanol in sequence for 10 min each to remove PMMA completely. After

rinsing under running DI water for 2 min, our sample with graphene on it was baked at 70 ℃ for 2 hours again.

Table 1 Polishing process details.

Abrasive suspension	Wheel Speed	Abrasive feed rate	Time
9 micron Diamond Suspension	50 rpm	1 drop/ 5 sec	20 min
1 micron alumina abrasive suspension	50 rpm	1 drop/ 10 sec	20 min
0.05 micron alumina abrasive suspension	50 rpm	1 drop/ 15 sec	20 min
colloidal silica suspension (0.02 ~ 0.06 micron)	50 rpm	1 drop/ 5 sec	20 min

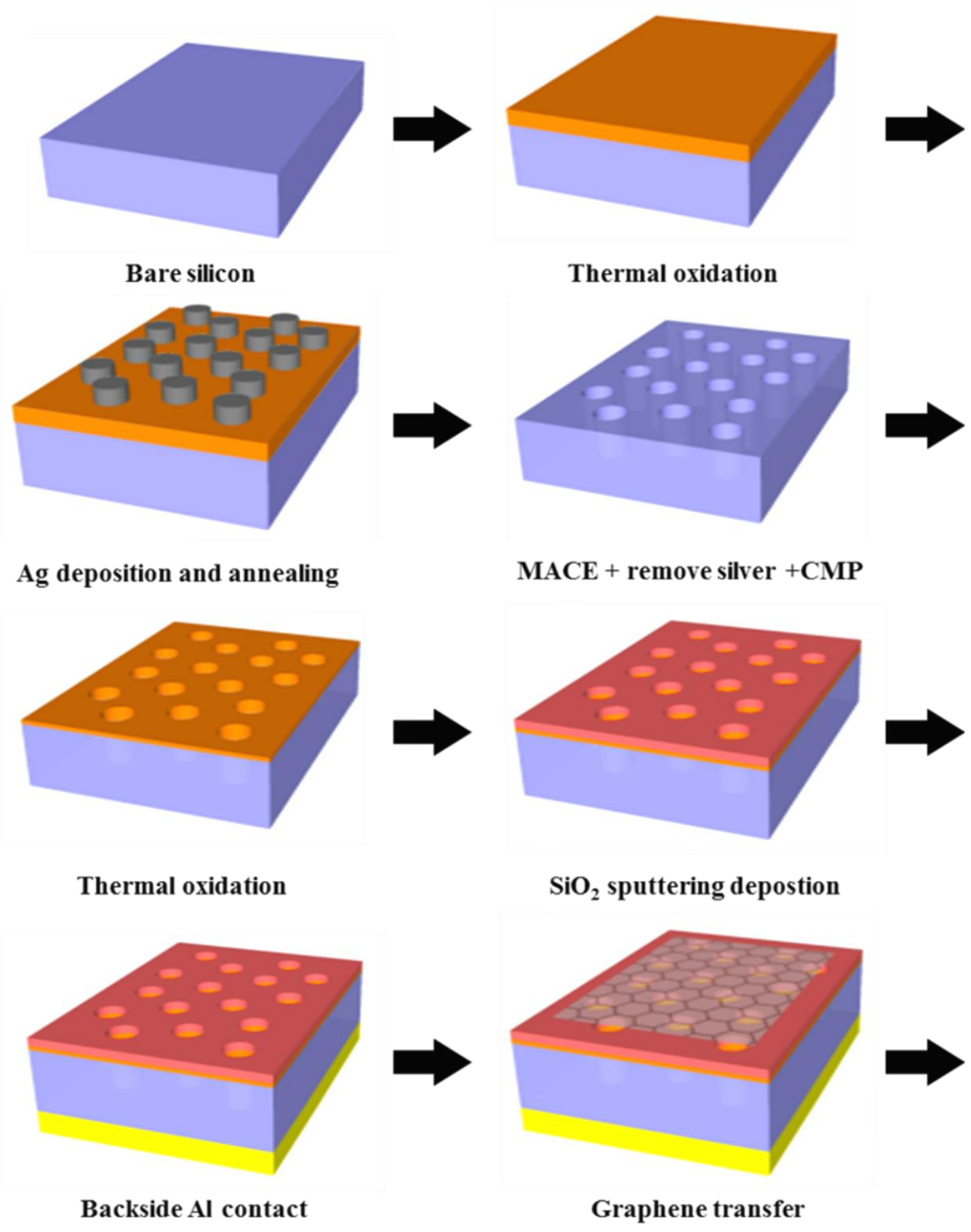


Figure 2 Scheme of overall fabrication process.

2.2 NANO-CHANNELS FORMATION ON SILICON

2.2.1 Introduction of metal-assisted chemical etching of silicon

Metal-assisted chemical etching (MACE) is a promising method in silicon nanofabrication. As a simple, non-lithographic process, MACE can create high-aspect-ratio nano-channels of sub-100nm-diameter and greater than several micron length. Usually a mixed solution of HF and oxidant such as H_2O_2 is used as etchant. Oxidants can generate holes through oxidizing reaction, which is also called cathode reaction. Hydrogen peroxide is the most commonly used oxidant in MACE. The reduction of H_2O_2 will generate hydrogen and holes:

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+$$

$$2H^+ \rightarrow H_2\uparrow + 2h^+$$

With the help of metal, oxidizing reaction will be accelerated. Therefore there will be more holes at the surface of the metal. Holes then diffuse through metal and are injected into the silicon under the metal. In this way silicon is oxidized:

$$Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

$$Si + 4HF_2^- \rightarrow SiF_6^{2-} + 2HF + H_2\uparrow + 2e^-$$

$$Si + 2H_2O_2 \rightarrow SiO_2 + 4H^+ + 4e^-$$

Silicon oxide created at the interface of metal and silicon is easily etched away by HF, which hardly attacks silicon:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

As a result, the silicon beneath the metal is dissolved much faster than the bare silicon parts and the metal sinks into the substrate, forming pores or wires. The shapes of these structures created depend dramatically on the initial status of the metal [10] [15].

It has been reported that etching direction (nano-channel direction) changes during the MACE process. The most acceptable explanation is that the difference in bond strength and silicon atoms density in different plane will result in a certain preferred etching direction. The etchant composition and noble metal coverage are expected to have an influence on etching direction.

When using (100) silicon substrate, etchant with low HF/H_2O_2 ratio will etch along the <100> direction, which has the lowest atom density, whereas increasing the volume of HF will allow etching direction moving towards the plane with larger atom density such as <110> even <111> [16]. For metal composed of small size individual particles and low particle density on (100) silicon, the preferred etching direction is <100> direction, both in vertical and horizontal directions. If we increase the particle density of the catalyst up to 70%, the etching direction orients to the vertical <100> direction only. More conclusively, if the catalyst on the substrate is interconnected and the average thickness is smaller than the average diameter of individual particle, the etching direction is always perpendicular to the surface [17]. The nanostructure and surface roughness of silicon after etching is different with or without stirring during etching: Bai et al. found that stirring the solution will lead to zigzag silicon nanowires while steady etchant

creates straight wires. The stirring will accelerate the evaporation of H_2 generated during etching, altering the etching direction towards different crystallographic directions [18].

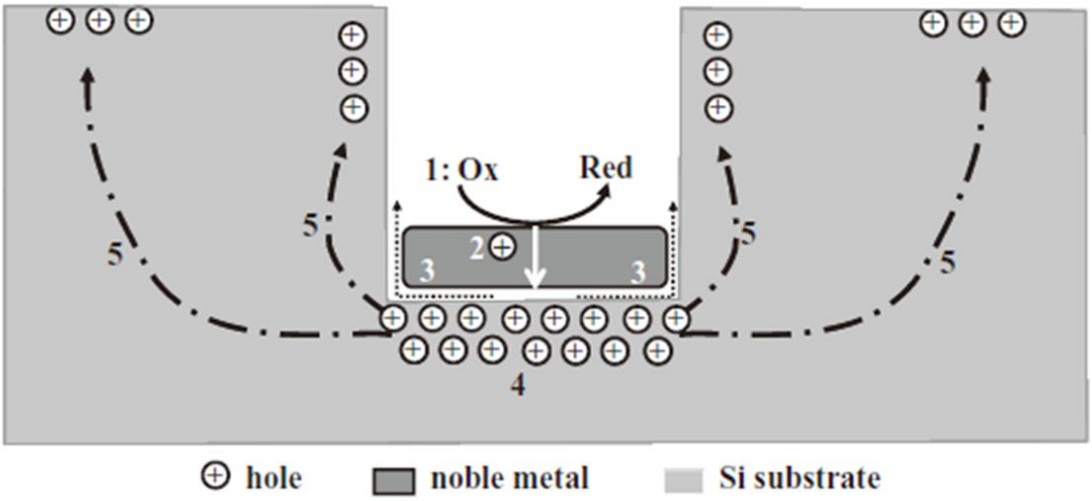


Figure 3 Scheme of overall processes during metal-assisted chemical etching. Step 1: cathode reaction occurs faster at the surface of the metal; step 2: holes are generated, diffusing through metal and then injected into the Si under metal; step 3: silicon is oxidized and is dissolved at the interface with metal by HF; step 4: hole density at the interface of silicon and metal is the largest. Thus silicon under metal is etched faster and metal sinks to the bottom of the channels; step 5: holes diffuse to the wall so the wall might be etched and form porous silicon. [15]

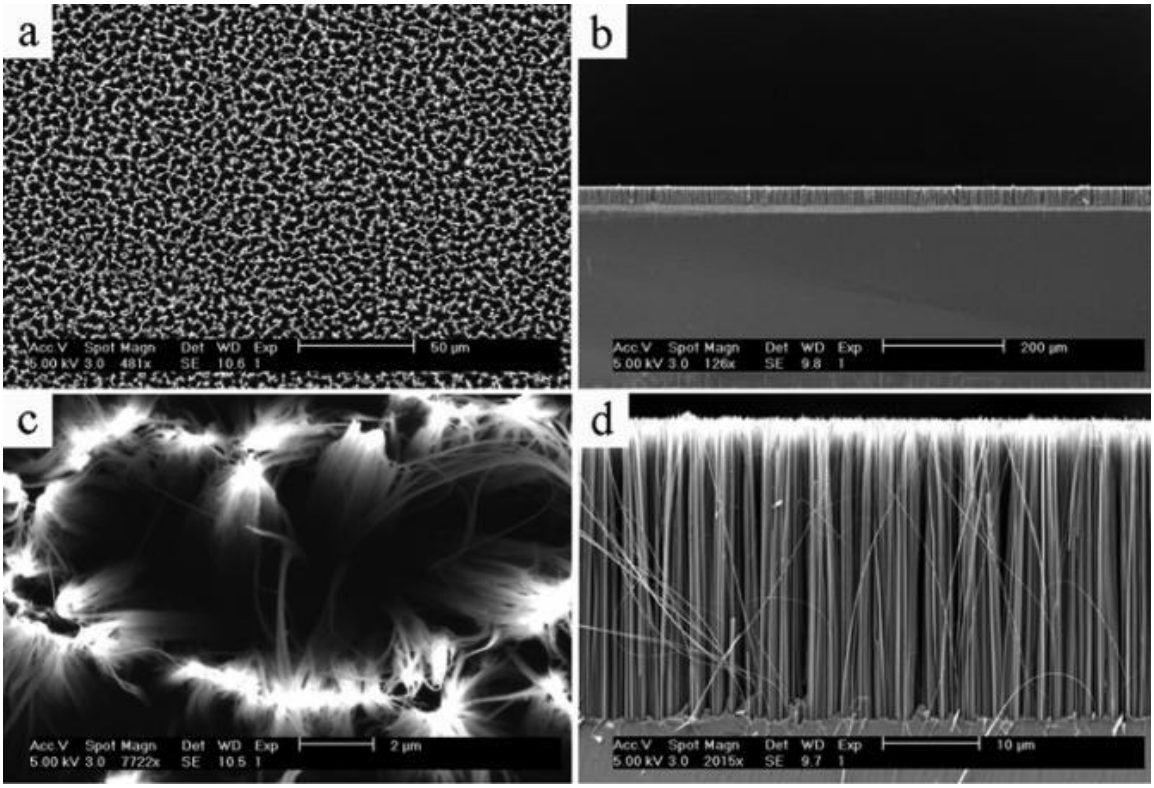


Figure 4 SEM images of silicon nanowires arrays prepared on p-Si(100) wafer with resistivity of 7-13 Ω·cm [19].

2.2.2 Self-organized silver nano particles

As mentioned in 2.2.1, the shape and surface morphology of the structure created by MACE mainly depend on the initial structure of the metal deposited on the silicon. In this work we have discovered that the silver-assisted chemical etching on silicon with a thin oxide layer provides smoother surface with more uniform channel dimensions, which would be beneficial to device application. See Figure 6 for plan view and Figure 7 for cross section image. Tracing back to the silver as-deposited on substrate, the self-organized silver particles have different density and particle size on silicon with and without oxide (Figure 5).

As-deposited silver film with mass thickness under 10 nm exists as a discontinuous film, comprising metal nano-particles with irregular shape and size. An annealing process has a tendency to induce coalescence of adjacent islands, forming larger size particles/islands. Annealing also induces metal islands to ball-up, especially when the metal has low melting temperature and the underlying surface does not provide good adhesion (wetting). In this work the annealing temperature was designed to be much lower than 960 ℃, which is the melting point of Ag, so no evaporation will occur during annealing process.

In our experiments (Figure 5), the as-deposited silver film (with mass thickness of 5 nm) on bare silicon shows surface coverage of ~43%, with average particle diameter of 15 nm and particle density of ~2500 islands per μm^2. After annealing, the surface coverage decreased to 38%, and average particle diameter slightly increased to 17 nm and the particle density decreased to ~1600 per μm^2. The as-deposited silver film (with mass thickness of 5 nm) on 38 nm silicon dioxide shows surface coverage of ~38%, average particle diameter of 13 nm and particle density of ~2700 islands per μm^2. After annealing, the surface coverage decreased to 34%, average

particle diameter slightly increased to 15 nm and the particle density decreased to ~2000 per μm^2. All the data are calculated with the help of ImageJ Toolbar.

In both cases, the average particle size slightly increased after annealing, mainly because of the coalescence of adjacent small islands. The particle density decrease after annealing also confirms that larger particles are formed through coalescence. The decrease of total surface coverage indicates that the average vertical thickness of silver particles increased (the nano islands raised up) since there is no mass loss during annealing.

Romanyuk et al. discovered that the bombardment of argon ions with low energy on silicon oxide surface would cause oxide reduction and create of surface vacancies. These vacancies become a nucleation site when depositing a silver film, which means longer time of bombardment, would lead to higher density of silver particles. Also silver on reduced oxide surface tends to start nucleation faster and has lower resistivity due to the high crystallinity [20]. Thouti et al. prepared a set of silver thin film (less than 12 nm) annealing at different temperature. As the mass thickness of silver thin film increases, the particles start to connect with adjacent ones and become anomalous in shape and larger in size. When increasing the annealing temperature, the surface coverage decreased and particle size increased, which well corresponds to our results [21].

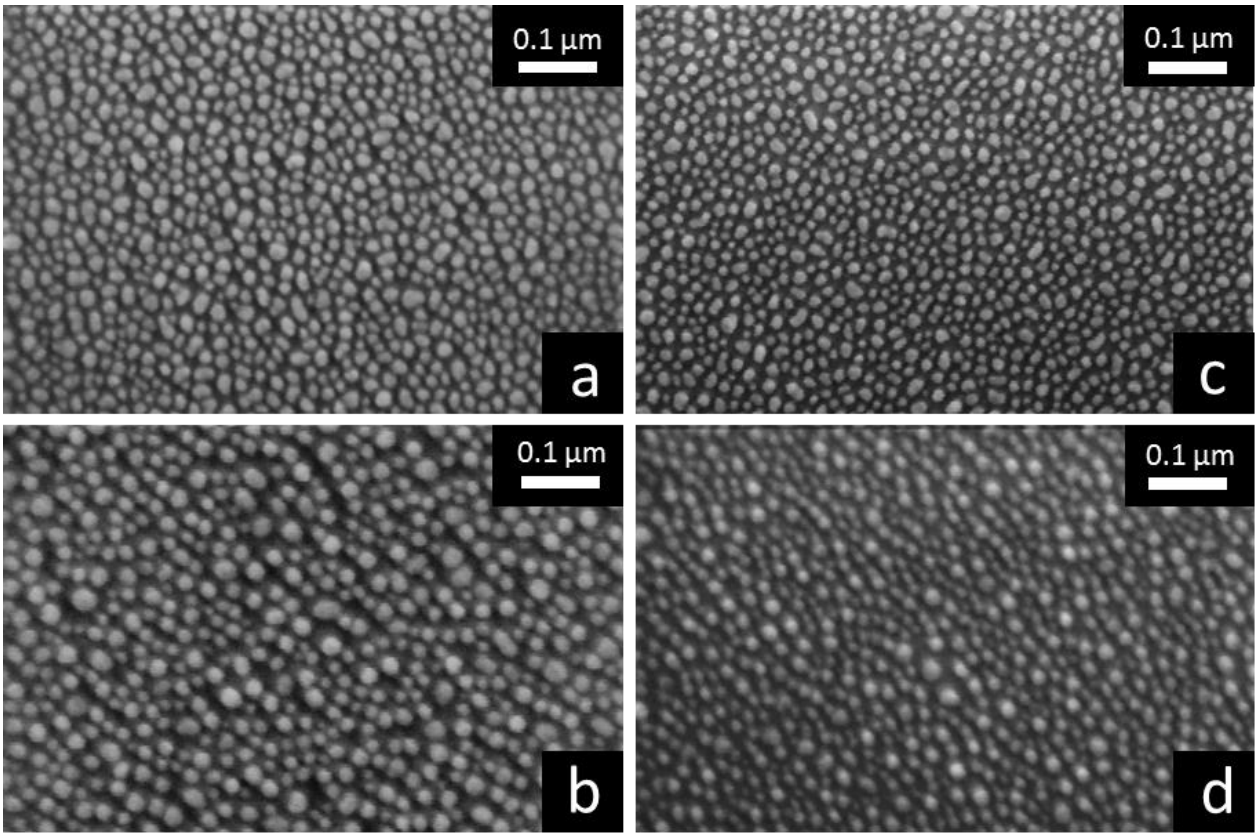


Figure 5 SEM image of 5-nm silver on top of n-type silicon substrate: (a) as deposited (b) after annealing in nitrogen ambient for 30 minutes at 250 ℃. 5 nm silver on top of n-type silicon substrate with 38 nm silicon oxide: (c) as deposited (d) after annealing in nitrogen ambient for 30 minutes at 250 ℃.

2.2.3 Thin oxide layer effect on silver-assisted chemical etching

We have investigated the effects of adding a thin oxide layer on metal-assisted chemical etching of nano-channels in Si. Samples with or without an oxide (38nm thickness) were etched for 9 min or 8 min, respectively. Comparing Figure 6 (a) and (b) with Figure 6 (c) and (d), we can observe better (smoother) surface morphology from the samples with oxide. The channel diameter is measured to be ~50 nm with the channel depth reaching over 4 μm depth for the given etching time (9 min). The channel density is also lower in samples with oxide. The randomly distributed small-size holes near channels are caused by the direction change during etching (Figure 7 (b) and (d)).

Silver nano-particles on silicon dioxide have smaller lateral dimensions and surface coverage both before and after annealing, compared to those on bare silicon (Figure 5). During silver-assisted chemical etching process, two independent processes are considered to occur: adjacent particles can merge, reducing particle concentration/coverage; particles ball up, thickening the vertical dimension, but reducing the lateral dimensions. Being insulator the transport of holes through an oxide layer is expected to be less than through Si. This will impede/suppress the channel etching process catalyzed by small size Ag particles and only the ones with larger particles will make through the oxide layer. The presence of a thin oxide layer has the effect of filtering off/blocking the channel etching by smaller size particles. This leads to a reduced surface coverage and therefore reduced surface roughness of Si (Figure 6 and Figure 7).

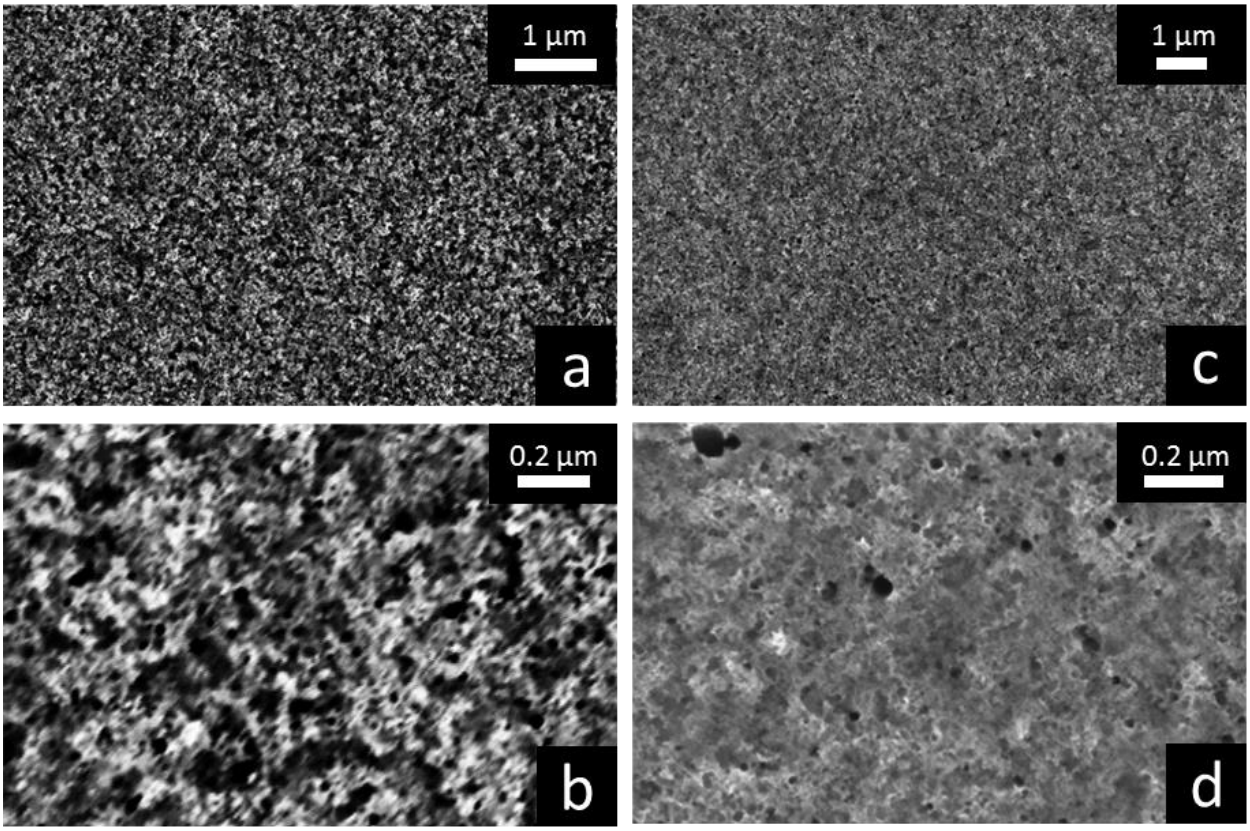


Figure 6 SEM plan view image for silver-assisted chemical etching. 8 minutes on bare silicon (a) and zoom in (b); 9 minutes on silicon with 38 nm thin silicon dioxide (c) and zoom in (d).

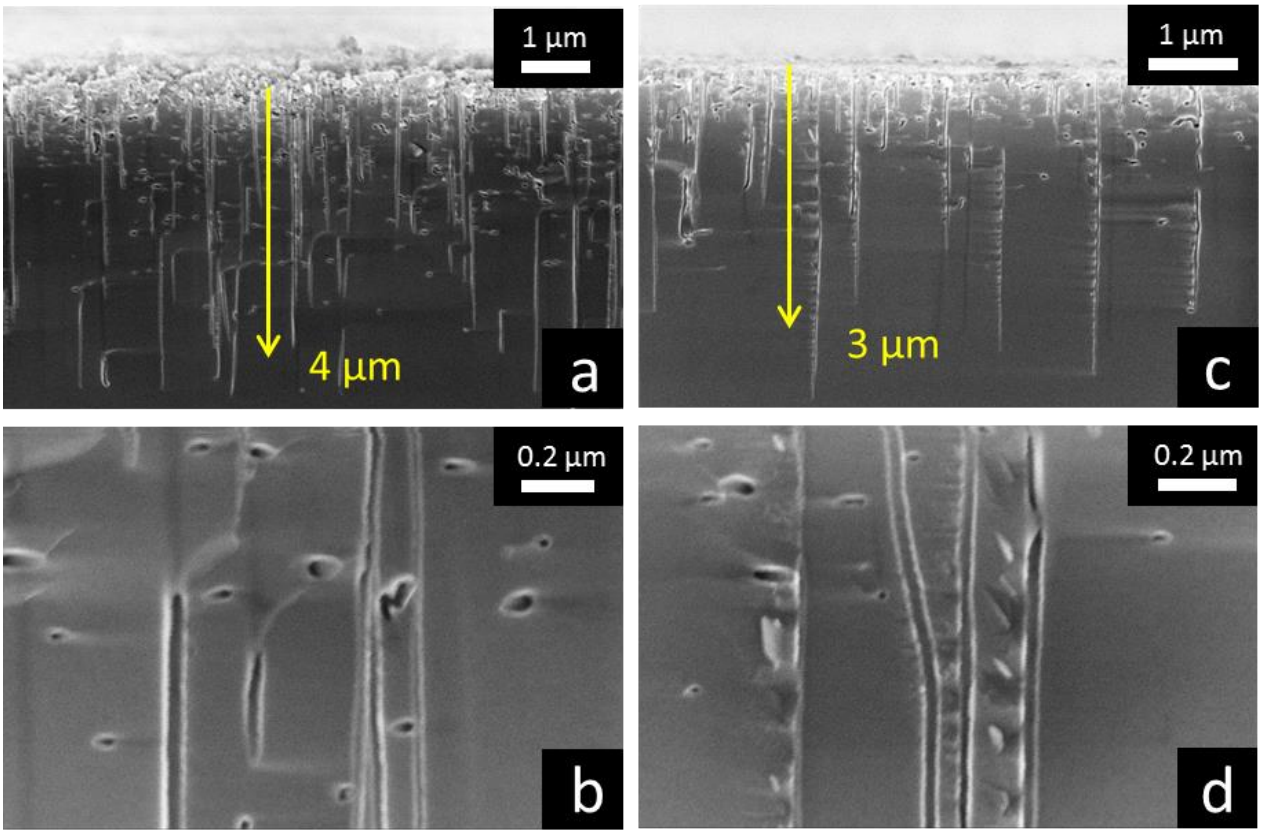


Figure 7 SEM cross section view image for silver-assisted chemical etching. 8 minutes on bare silicon (a) and zoom in (b); 9 minutes on silicon with 38 nm thin silicon dioxide (c) and zoom in (d).

2.3 CHEMICAL MECHANICAL POLISHING

We have discussed the beneficial effect of introducing a thin oxide layer on reducing the roughness of nano-channel-etched Si surface. The cross-section image of channel-etched substrate, however, reveals presence of a high concentration of short channels in the top part and long, uniform channels extend deep at a much lower concentration. With our interest in utilizing the long channels we have decided to employ a chemo-mechanical polishing process to remove the top part of channel-etched substrate.

Chemical mechanical polishing (CMP) is a polishing process involving more chemical reaction compared to traditional mechanical polishing processes and is widely used in integrated circuit fabrication as a planarization method. Figure 8 shows the scheme of chemical mechanical polishing. A polishing plate with polishing cloth or abrasive film on top will spin at a fixed rate. Abrasive slurries or suspension will be fed at the same time on to the polishing pad. The sample is mounted using vacuum or mounting wax facing down on sample carrier which is usually rotating in the opposite direction of polishing plate. Material removal rate is determined by the wafer-pad relative motion and interfacial pressure. Preston's equation demonstrates this relationship: $r = kPV$. Where r is removal rate, constant k is called Preston coefficient, P is interfacial pressure and v stands for relative velocity.

Non-uniformity in the polishing process is caused by the different pressure and speed applied across the wafer surface. The hydrodynamic effect of slurry, the visco-elastic

deformation of polishing cloth and oscillation of both sample carrier and polishing plate will also affect uniformity.

The abrasive material is a mixture of abrasive particles and chemical solution or water. It will improve the polishing quality and tune the removal rate through different chemical reaction, varying pH value and particle size.

Since the CMP process involves various organic and inorganic materials, which are a contamination source in IC processing, it is critically important to apply a post-CMP cleaning process to remove any impurities remaining on the sample. A cleaning process after each polishing session is also necessary to minimize former abrasive material residue. In our CMP process, mechanical cleaning, such as brush scrubbing on polishing cloth and facing-down ultrasonic bathing for sample, are done every time we change the abrasive suspension. Samples were immersed in acetone, methanol and DI water in ultrasonic bath for 20 minutes in sequence to further remove chemical contamination.

Figure 9 shows SEM images of silicon substrate with nano-channels before and after polishing. From the cross section view Figure 9 (a) and (d) we can see decent improvement of surface roughness: the thickness of bumpy and porous layer reduced from ~1.5 μm to less than 0.5 μm. The polishing process removed ~1 μm thickness of rough part from the surface and thus the channel length was reduced from over 4 μm to 3 μm. The plan view image confirmed improved surface quality. In Figure 9 (b) and (c) the surface looks extremely non-uniform in color, whereas after polishing we can distinguish the channel position under a uniform color background (Figure 9 (e) and (f)). The channel density is ~ 40 per μm^2, which is significantly lower than the silver particle density 2000 per μm^2. The short white lines appearing parallel to

the surface are the channels created as the etching direction turned 90 degree to the horizontal direction.

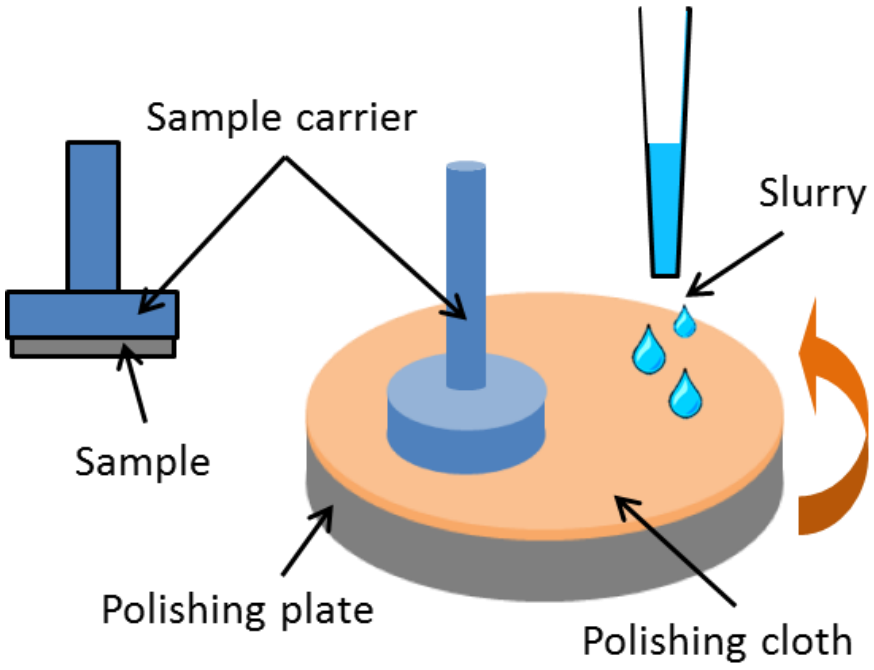


Figure 8 Scheme of chemical mechanical polishing.

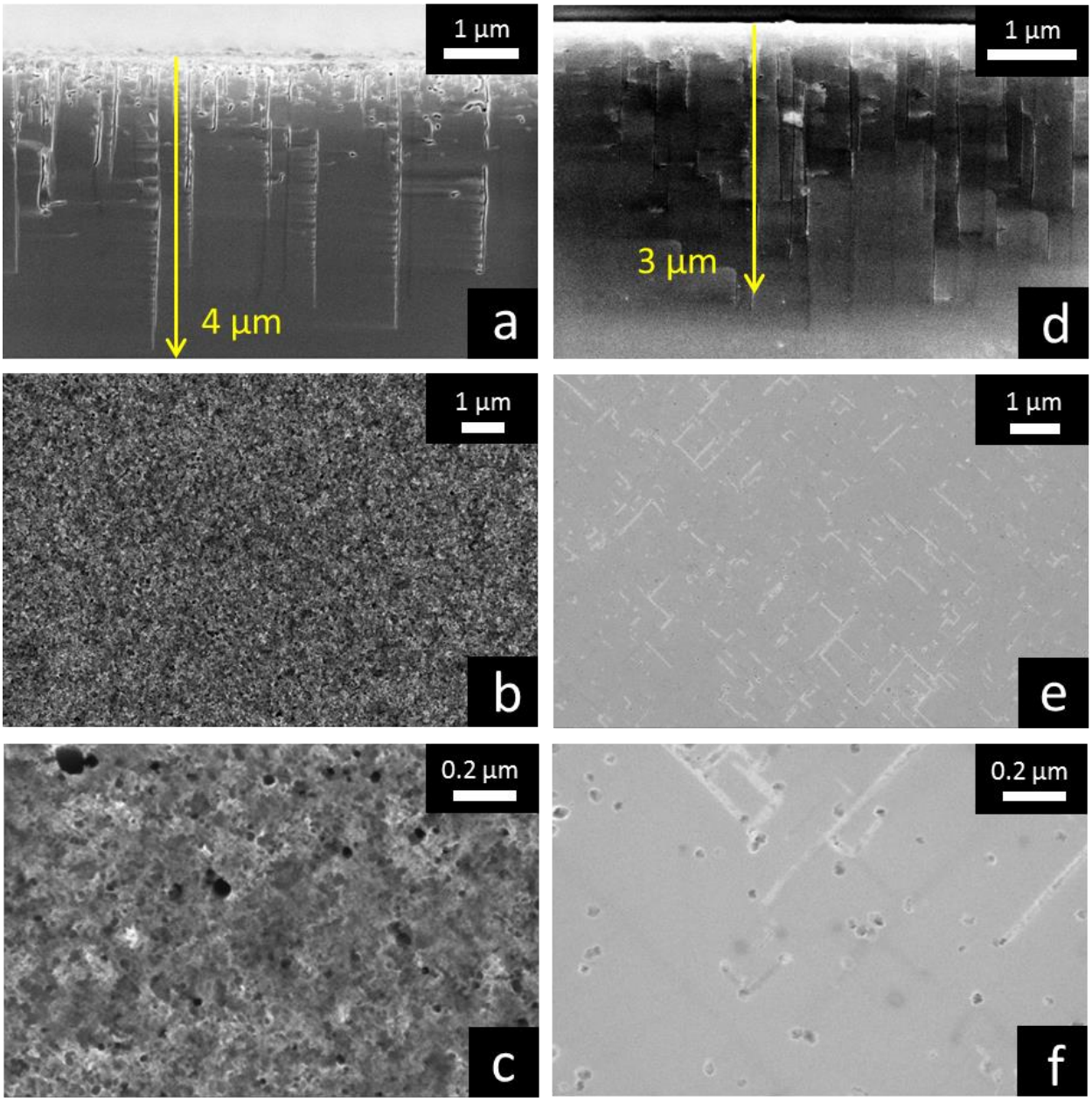


Figure 9 SEM image for samples before CMP (a, b, c) and after CMP (d, e, f). (a) and (d) : Cross section view; (b, c): Plan view of surface before polishing (after channel formation); (e, f) : Plan view of surface after polishing.

3.0 OPTICAL CHARACTERIZATION

3.1 ANGULAR SPECTRUM MEASUREMENT

Reflection and refraction will occur at the interface of different media as an incident beam hits the surface. Assume incident and reflected waves propagate in medium 1 (refractive index of n_1) and transmitted wave in medium 2 (index n_2). Applying the phase matching condition of three waves at the interface, we obtain

$$n_1 sin\theta_i = n_1 sin\theta_r = n_2 sin\theta_t$$

Note that the incident angle θ_i and the reflection angle θ_t are always equal. The relationship between incident angle θ_i and transmission angle θ_t is

$$\frac{sin\theta_i}{sin\theta_t} = \frac{n_2}{n_1}$$

Consider two perpendicular polarizations of incident wave: s-wave (TE wave) and p-wave (TM wave). Applying the boundary condition that both the electric and magnetic fields' tangential components are continuous at the interface, we will get the coefficients of reflection (r) and transmission (t), as well as the reflectance (R) and transmittance (T) :

$$\begin{cases} r_{TE} = \dfrac{n_1 cos\theta_i - n_2 cos\theta_t}{n_1 cos\theta_i + n_2 cos\theta_t} \\ t_{TE} = \dfrac{2n_1 cos\theta_i}{n_1 cos\theta_i + n_2 cos\theta_t} \end{cases}$$

$$\begin{cases} r_{TM} = \dfrac{n_1 cos\theta_t - n_2 cos\theta_i}{n_1 cos\theta_t + n_2 cos\theta_i} \\ t_{TM} = \dfrac{2n_1 cos\theta_i}{n_1 cos\theta_t + n_2 cos\theta_i} \end{cases}$$

$$\mathrm{R} = |\mathrm{r}|^2$$

$$\mathrm{T} = \frac{n_2 cos\theta_t |\mathrm{t}|^2}{n_1 cos\theta_i}$$

Brewster's angle (θ_B) is defined as the incident angle at which there is no reflection for TM wave:

$$\theta_B = \arctan\frac{n_2}{n_1}$$

Assume a light is incident from air to silicon or silicon dioxide: $n_1 = 1.0$ for air, at 633 nm wavelength $n_2 = 3.9$ for silicon, $n_2 = 1.5$ for silicon dioxide and $n_2 = 2.0$ for silicon nitride. The Brewster's angle for silicon, silicon dioxide and silicon nitride is 75º (Figure 10), 56 º (Figure 11) and 63 º, respectively.

For convenience of analysis, the nano-channels formed in silicon can be approximately considered as a random 2D grating. At the interface of air and silicon, the phase of incident light and transmitted light should match to satisfy the conservation of momentum. Figure 12 shows the wave vector phase matching diagram when light incidents from air to silicon:

$$K_i + K_g = K_t^{(m)}$$

$$K_i = k_0 \sin\theta\,, \qquad 0 < \theta < \frac{\pi}{2}$$

$$K_g = m\,\frac{2\pi}{d} = m\,\frac{\lambda}{d}k_0\ , \qquad k_0 = \frac{2\pi}{\lambda}\ and \quad m = 0, \pm 1, \pm 2, \cdots$$

Where λ is incident wavelength, θ is incident angle, d is a grating period and m is the order of grating vector.

Nano-channels have a density of 20 per μm^2 with diameter of 50 nm, corresponding to an average grating period of 230 nm. For λ = 633nm, d = 230 nm, $K_i + K_g$ is always greater than k_0 when m takes a positive value and $K_i - K_g$ is always less than k_0 when m takes a negative value. Therefore there is no grating diffraction in this sample structure.

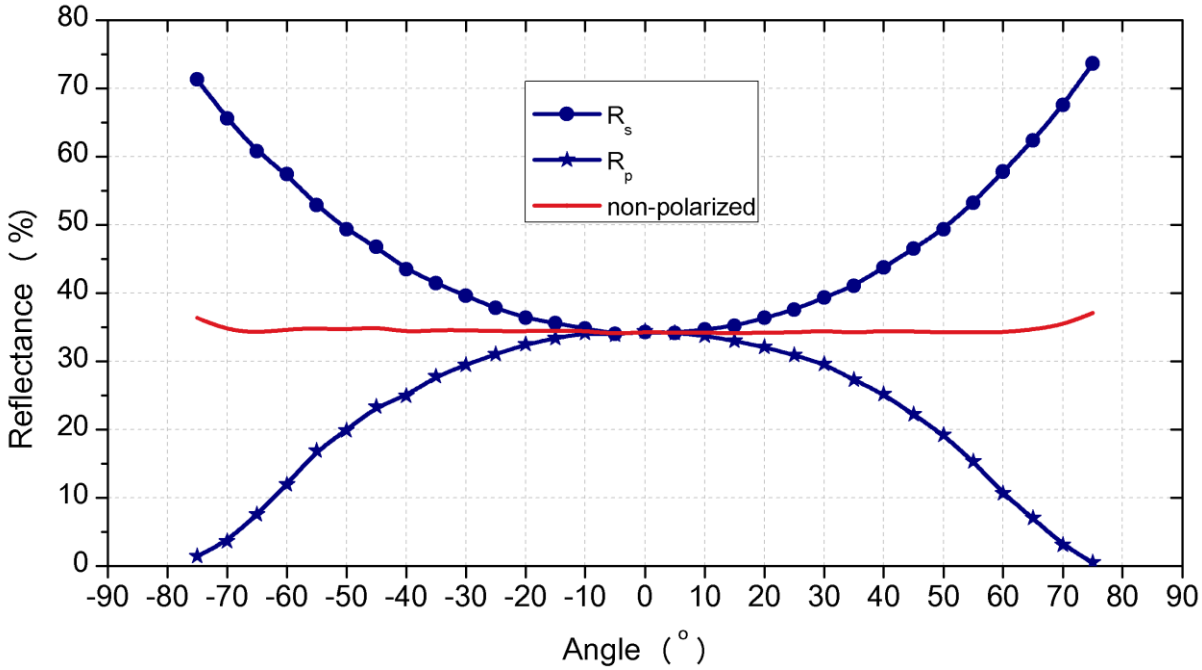


Figure 10 Angular dependence of reflectance for cleaned bare silicon.

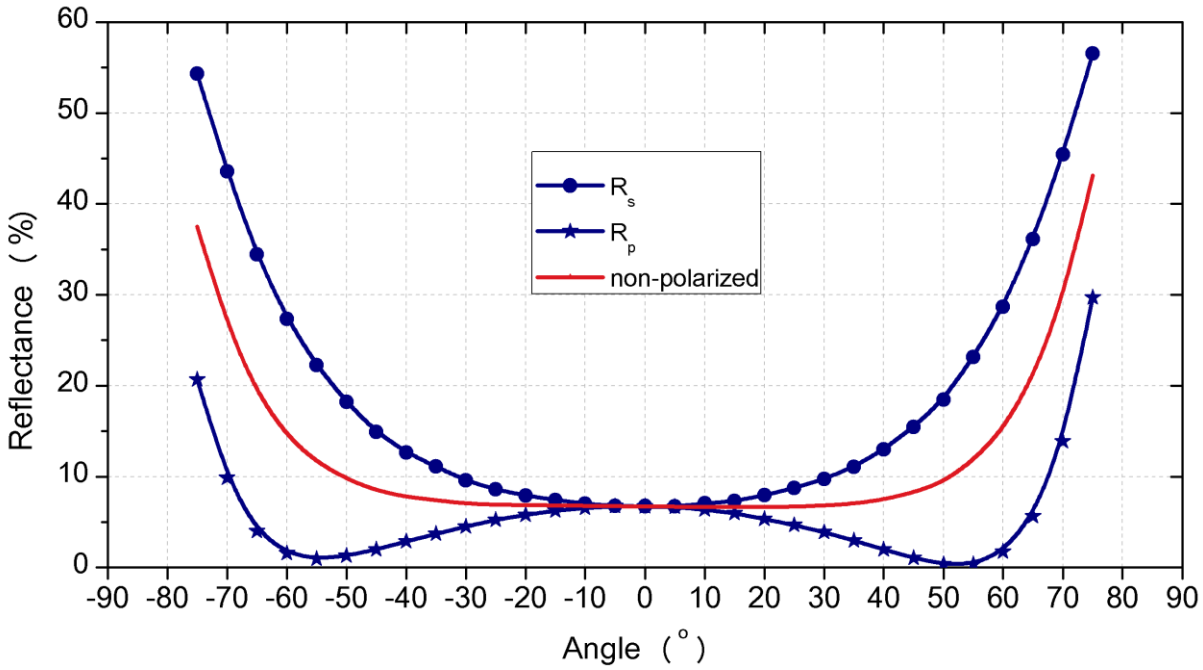


Figure 11 Angular dependence of reflectance for quartz (silicon dioxide) with thickness of 500 μm.

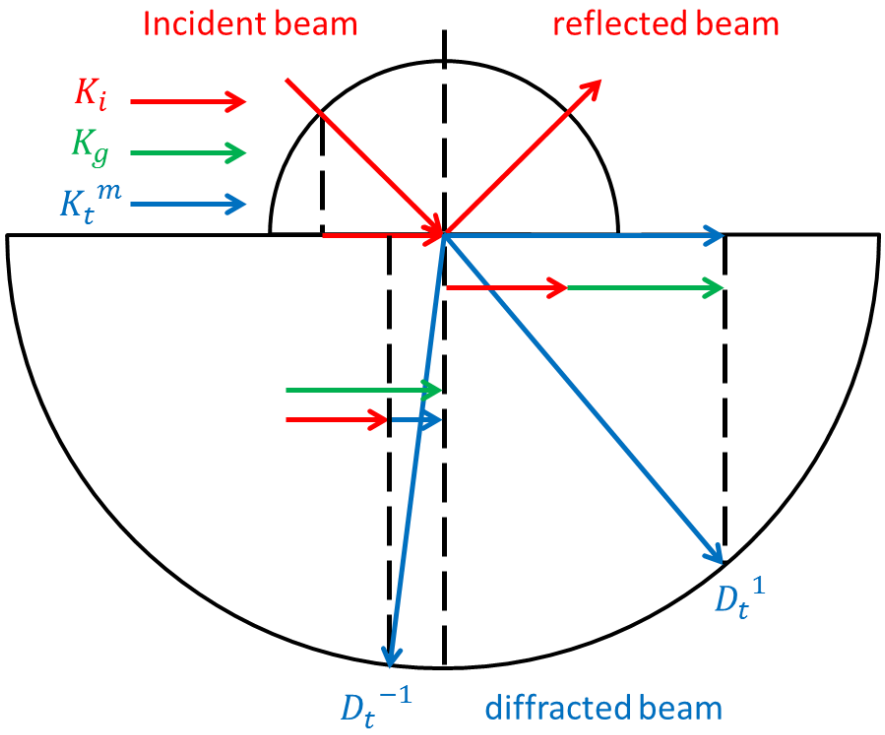


Figure 12 Wave vector phase matching diagram at the interface of air and silicon.

Specular reflection spectra are obtained along two perpendicular directions for both TE and TM polarizations (also known as s-polarization and p-polarization) of incident light.

Figure 13 shows the angular reflectance of silicon substrate with nano-channels characterized right after metal-assisted-chemical-etching (MACE). The reflectance at normal incidence is characterized to be 0.4 %. The extremely low reflectance results in apparently dark color of Si surface, which is commonly referred to “black silicon”.

Figure 14 shows the angular reflectance of silicon substrate with nano-channels characterized after chemical mechanical polishing (CMP): the reflectance at normal incidence now increased to 20.0 %. Compared to the reflectance of 34.3 % on bare silicon at normal incidence, the nano-channels reduced the overall reflectance. The nano-channels serve as vertical dipoles which radiate light in glancing angles, which will be further discussed in section 3.2. Figure 15 presents the angular dependence of reflectance of silicon substrate with nano-channels before and after chemical mechanical polishing (CMP), comparing with bare silicon reference.

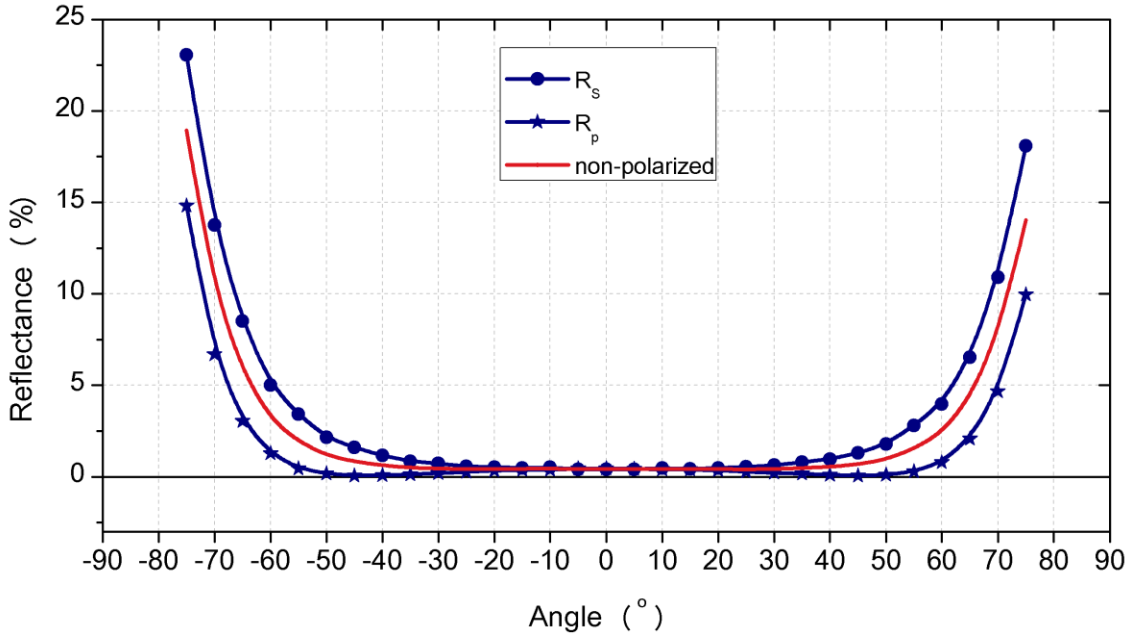


Figure 13 Angular dependence of reflectance of silicon substrate with nano-channels right after metal-assisted-chemical-etching (MACE).

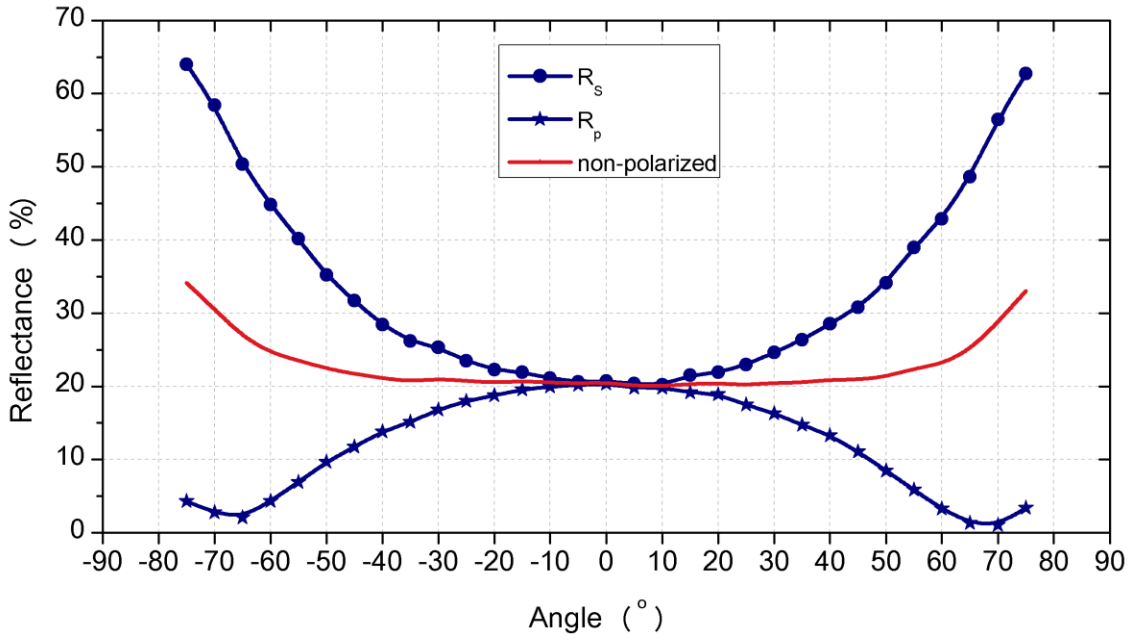


Figure 14 Angular dependence of reflectance of silicon substrate with nano-channels after chemical mechanical polishing (CMP).

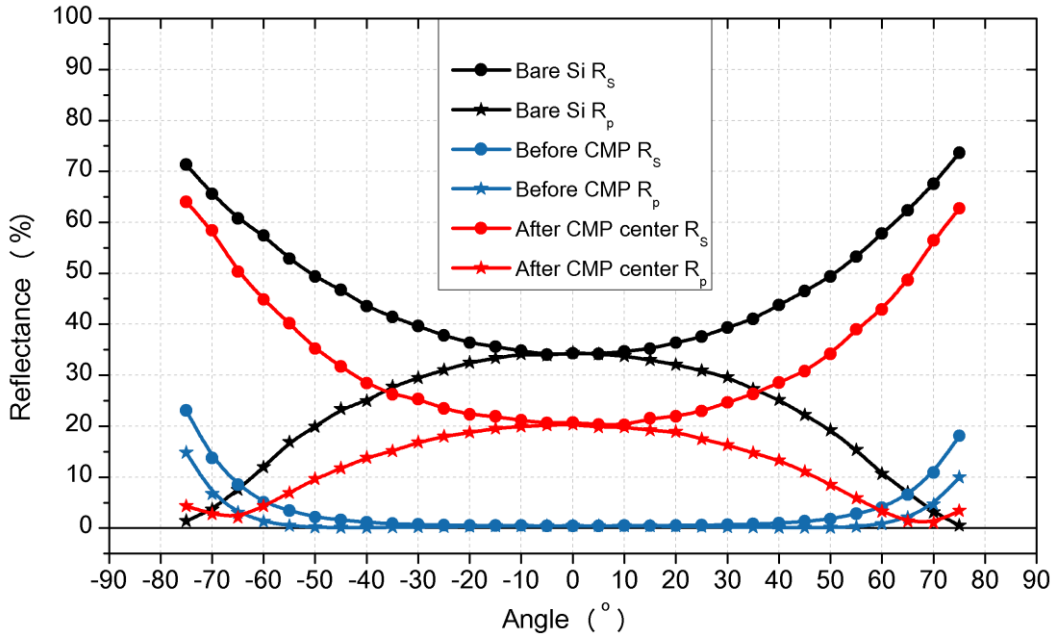


Figure 15 Angular dependence of reflectance of silicon substrate with nano-channels before and after chemical mechanical polishing (CMP), comparing with bare silicon reference.

3.2 INTEGRATING SPHERE MEASUREMENT

The nano-channel-etched Si surface is expected to make both specular and diffuse scattering of incident light. In order to characterize the spectral dependence of total scattered/reflected light we have employed an integrating sphere. An integrating sphere is an instrument with a spherically-shaped chamber with highly reflective inner surface. Any reflection occurring inside the chamber results in scattered reflection. The instrument integrates a light flux over a spatial domain, which means the light incident on any point of the inner surface is spread equally to all other parts inside the chamber. Therefore the influence of the original direction of light is highly reduced. The integrating sphere can be considered as a light diffuser, which conserves the total incident power but eliminates the original spatial information.

A nano-channel sample is attached facing inside the sphere, and the detector port collects a light signal transported through a fiber toward a CCD based spectrometer (Figure 16). The spectrometer is connected to computer with matching software BWTEK 3.27. The settings in the software BWTEK 3.27 are optimized to obtain maximum input signal without saturation: 25 ms integration time and average number of 50 are chosen. Tungsten light source has a broad spectrum from 350 nm to 2600 nm.

First a reference data is obtained by placing a highly reflective (> 97%) material (PTFE) at the sample port. PTFE is the same material as coated on the inside wall of integrating sphere. A dark scan is taken to measure the intrinsic noise of the system. The raw data is processed to produce reflectance value:

$$\text{Reflectance} = \frac{raw\ data - dark\ scaned\ data}{reference\ data - dark\ scaned\ data} \times 100\%$$

Figure 17 shows the reflectance of bare silicon at wavelength range 450 nm to 1050 nm measured by an integrating sphere, which has a reflectance of 25.6 % at 633 nm. Figure 18 shows the results of silicon with nano-channels before CMP, which has a reflectance of 3.85 % at 633 nm. Figure 19 shows the results of silicon with nano-channels after CMP, which has a reflectance of 15.73 % at 633 nm.

Comparing the reflectance measured by power meter (Figure 15) and by integrating sphere (Figure 20), the overall trend remains the same: after MACE the silicon surface becomes "dark" and CMP will recover part of the reflectance loss over a broad spectral range. But the results of two methods reveal a certain degree of discrepancy. For example, at 633 nm the reflectance values do not agree exactly. The power sensor method measures primarily specular reflection whereas the integrating sphere can measure both specular and diffused reflection. This may explain a big discrepancy observed with the nano-channel-etched sample (before CMP): 10 times larger reflectance by integrating sphere (3.85%), compared to the photodetector method (0.4 %). With more reflective samples, however, the integrating sphere produces ~74 % lower reflectance than the photodetector method. This might be explained by the intrinsic loss from the design of integrating sphere as well as the leakage in sample port. Overall this result confirms that CMP process significantly suppressed the scattering loss from the surface.

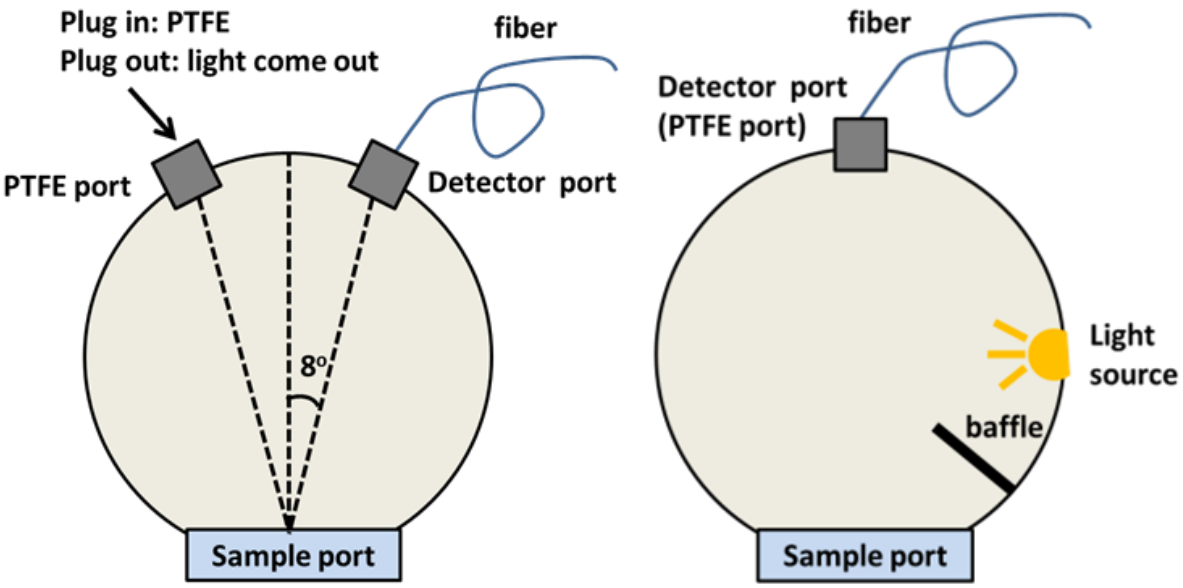


Figure 16 Scheme of reflectance measurement by integrating sphere.

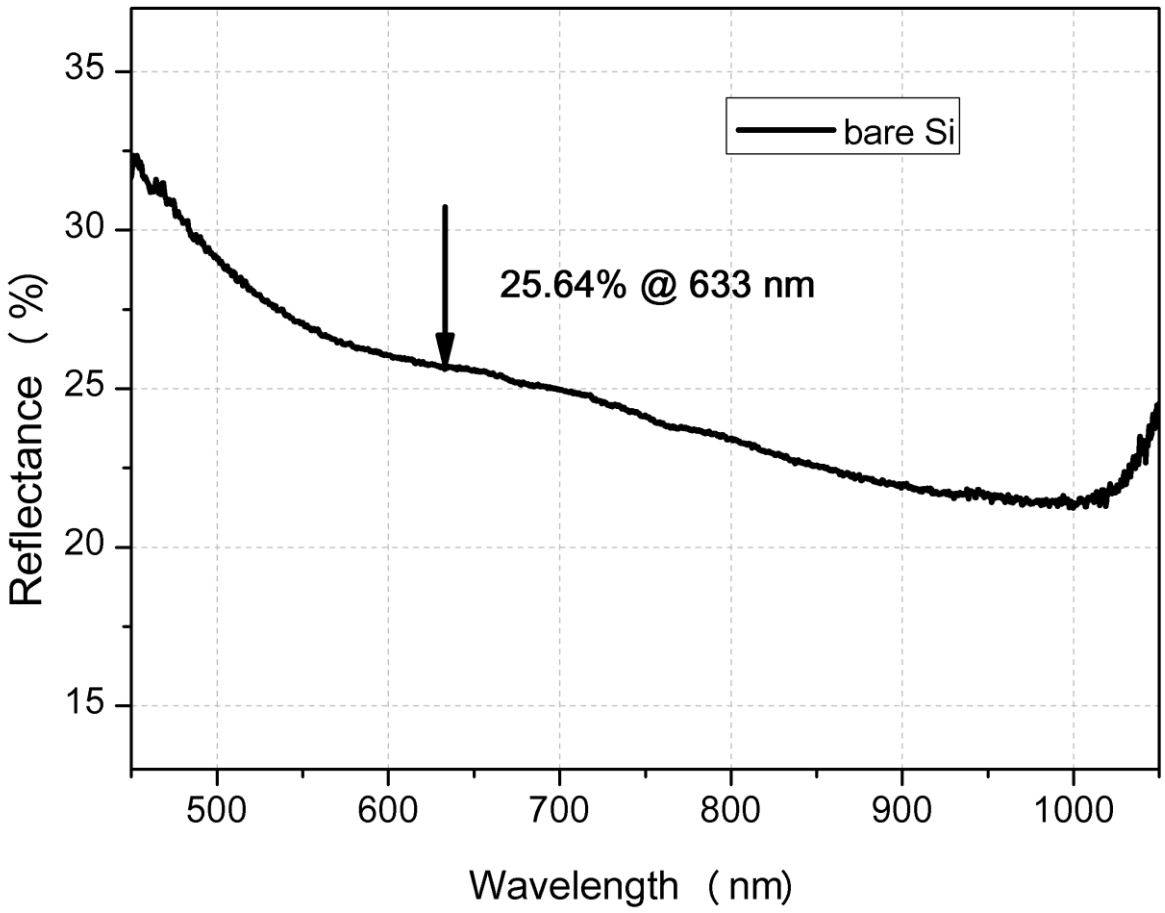


Figure 17 Reflectance of bare cleaned silicon measured by integrating sphere.

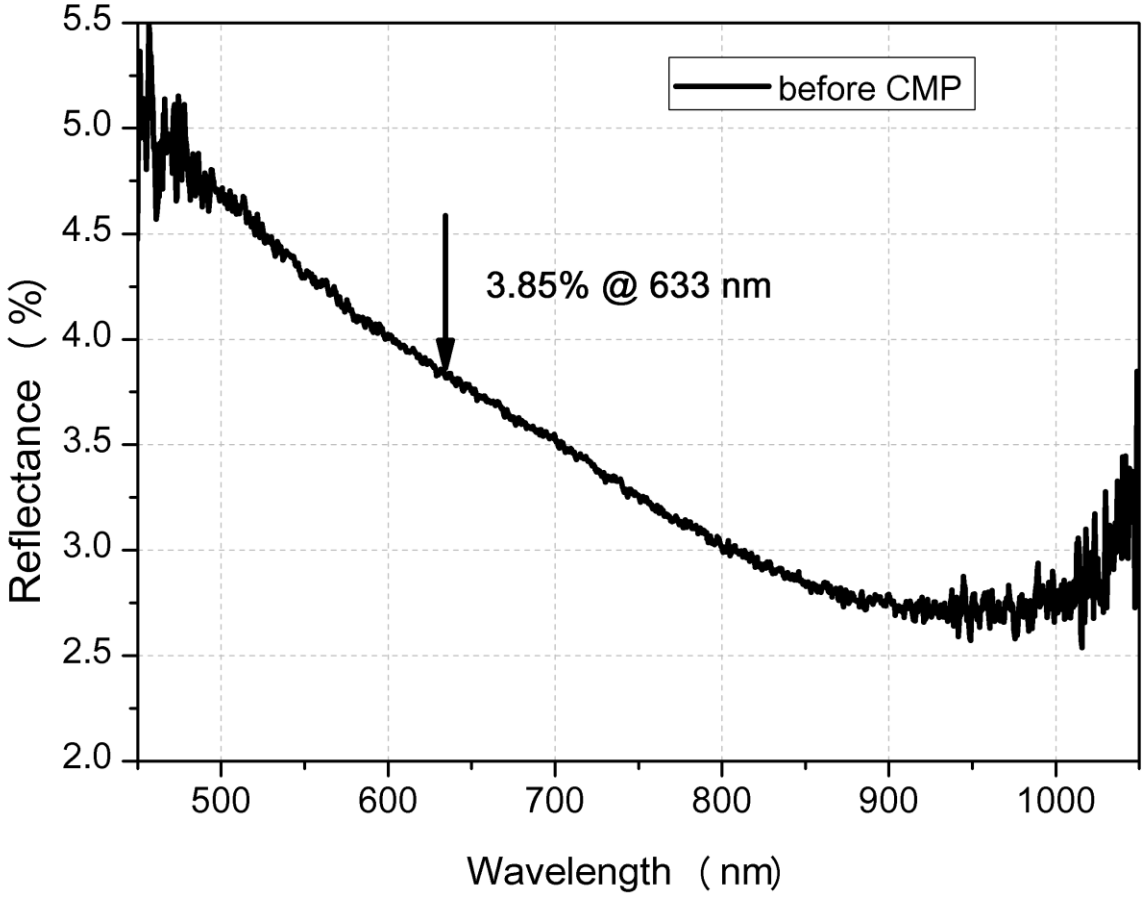


Figure 18 Reflectance of silicon with nano-channels before CMP measured by integrating sphere.

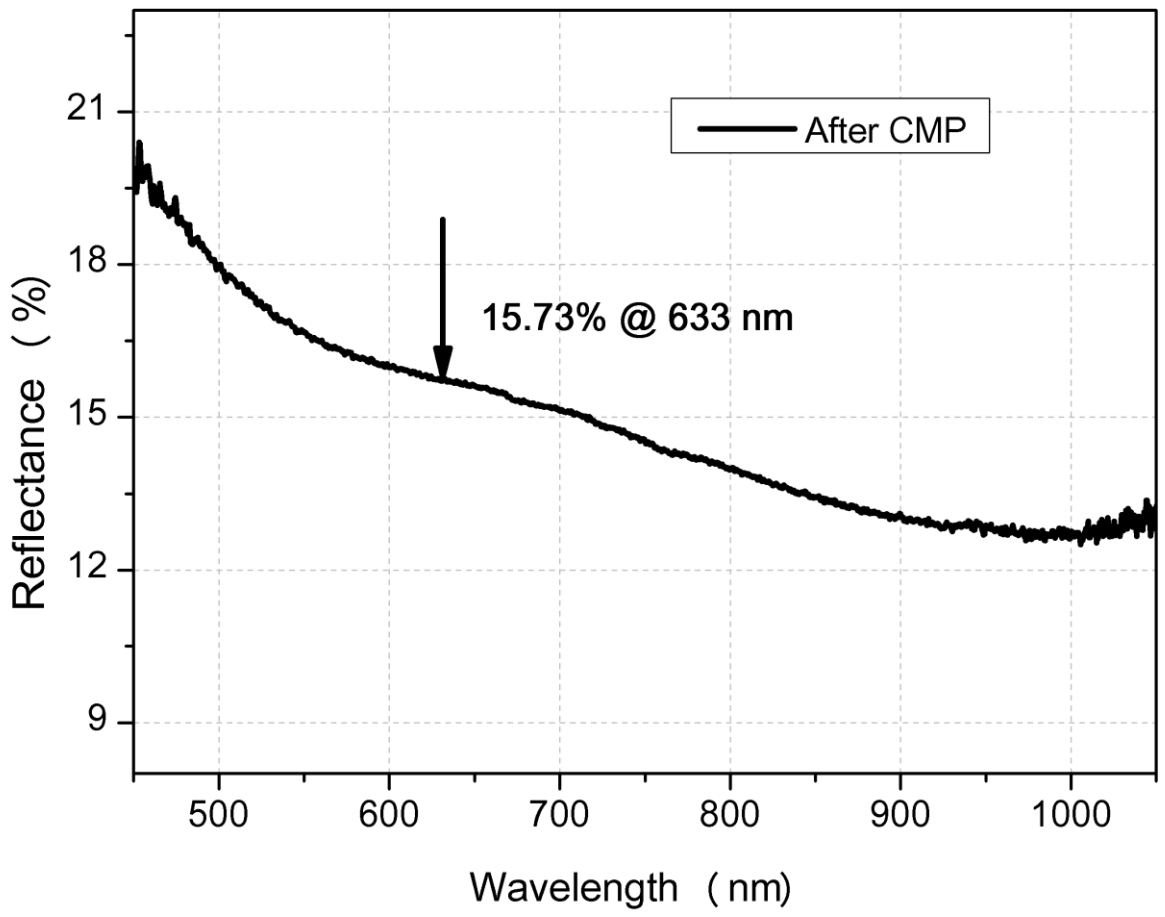


Figure 19 Reflectance of silicon with nano-channels after CMP measured by integrating sphere.

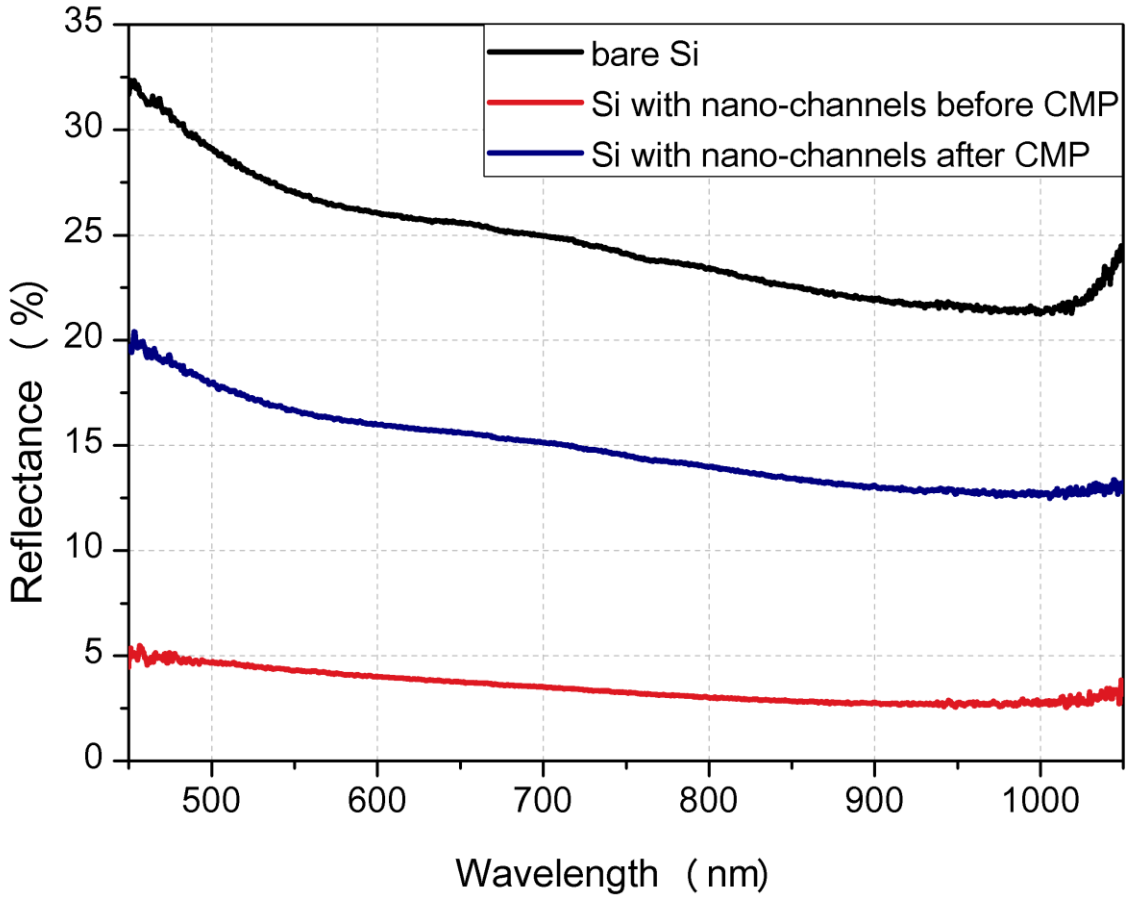


Figure 20 Reflectance of bare silicon, silicon with nano-channels before and after CMP measured by integrating sphere.

4.0 ELECTRICAL CHARACTERIZATION: DARK AND PHOTO RESPONSE

4.1 INTRODUCTION

4.1.1 MOS Structure and GOS structure

Metal-oxide-semiconductor (MOS) capacitor structure is a backbone of silicon microelectronics. The Si surface, when passivated by thermally grown oxide, can harbor a good quality two-dimensional electronic system (2DES). Under reverse bias an inversion channel can develop at SiO_2/Si interface, and this channel serves for carrier transport in MOS field-effect-transistor. Under illumination of light photocarriers are also generated in Si. With proper bias that provides depletion field around the interface, carrier separation occurs and photogenerated minority carriers can get trapped at the interface forming an inversion channel. In this study we have developed a graphene/oxide/nano-channel-etched Si (GOS) capacitor structure and investigated the photo detection properties. In this structure photocarriers are extracted through a thin oxide layer via tunneling process. Here graphene is used as a transparent conducting electrode. The nano-channel-etched Si surface is expected to provide an antireflection effect.

Figure 21 shows the energy band diagrams of MOS and GOS structures with n-type and p-type silicon: band bending occurs when Fermi level aligns. $q\Phi_M$ is the work function of metal, the minimum energy that an electron needs to gain to escape from metal surface. Aluminum has

work function of 4.1 eV. $q\chi_S$ (~ 4.05 eV) is the electron affinity of silicon [22]. $q\chi_{ox}$ (~ 0.9 eV) is the electron affinity of silicon dioxide. The band gap of silicon is 1.12 eV and of silicon dioxide ~8.5 eV. For n–type silicon with resistivity 20 to 60 Ω-cm, the Fermi level is at ~4.24 eV. For p–type silicon with resistivity 10 to 20 Ω-cm, the Fermi level locates at ~5.05 eV.

In the graphene/oxide/semiconductor (GOS) structure graphene replaces metal as a transparent conducting electrode. The Fermi level of intrinsic graphene $q\Phi_G$ is at Dirac point ~ 4.56eV and can be shifted by applying external electric field or chemical doping. However graphene transferred on substrate will be slightly p-doped, attributed to impurities remaining on graphene. This intrinsic doping can be recovered through thermal annealing in Ar ambient under temperature of 400 ℃ [23]. A shift of Fermi level from Dirac point will result in increased carrier concentration.

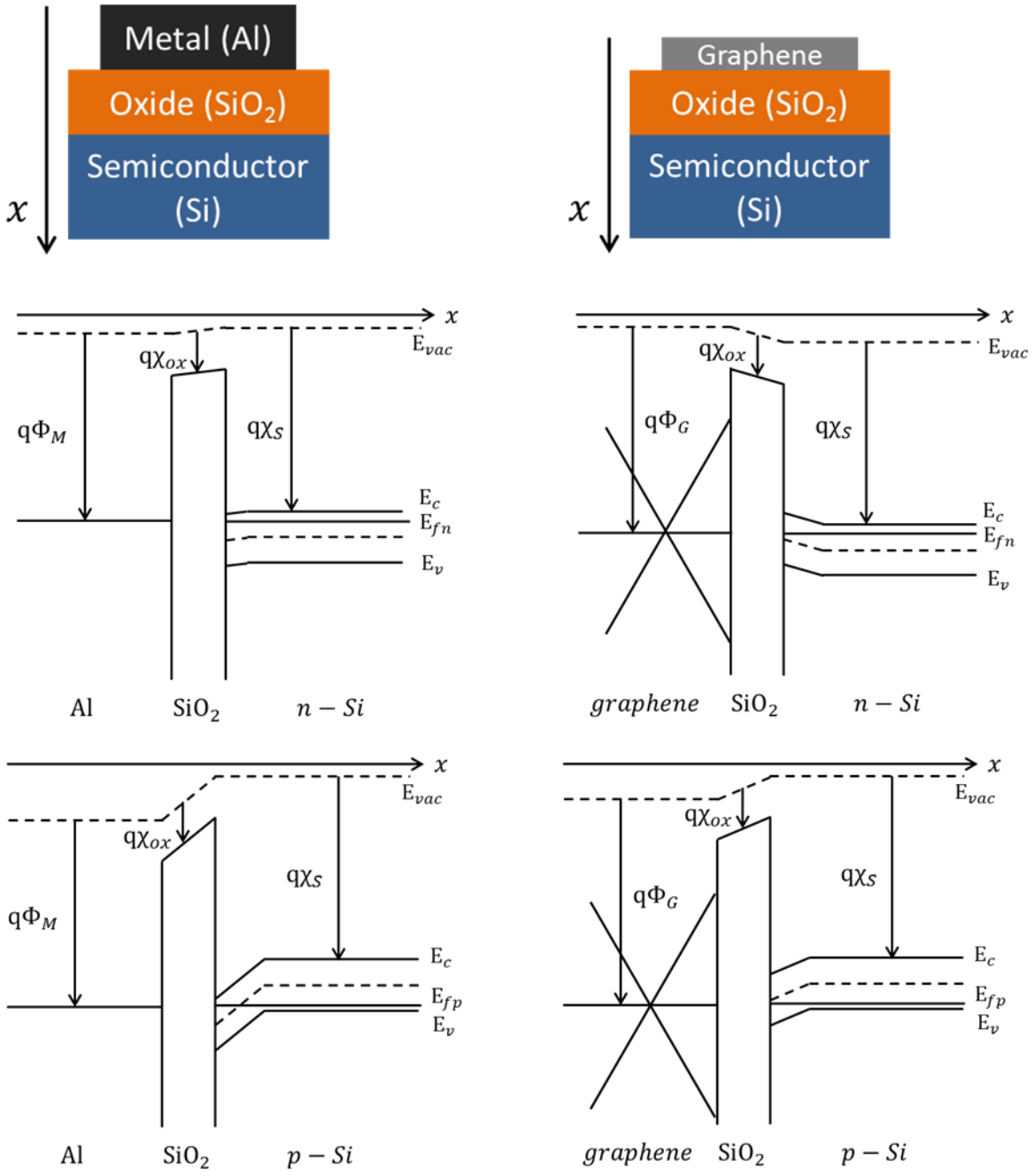


Figure 21 Energy band diagram for MOS and GOS structure on n-type and p–type silicon.

4.1.2 Electron emission and transport

Various (vertical) transport mechanisms are possible for carriers generated in MOS or GOS structure. Thermionic emission occurs when an electron absorbs enough thermal energy that exceeds work function. The current density of thermionic electron emission J_{th} is calculated according to Richardson-Dushman Equation:

$$J_{th} = -A_{th}T^2 exp\left(-\frac{\phi}{TB_{th}}\right)$$

Where T is temperature, ϕ is the work function, A_{th} and B_{th} are constants depend on material. J_{th} is exponentially proportional to the work function at power of 1.

Field emission is also called cold emission that, unlike the hot carriers generated in thermionic emission, the electrons are driven by electric field. Usually ultrahigh electric field is needed to create a triangular barrier for electrons to transport through quantum tunneling. The tunneling current density J_{FN} is calculated from Fowler-Nordheim equation:

$$J_{FN} = A_{FN}F^2 exp\left(-\frac{B_{FN}}{F}\right)$$

$$A_{FN} = \frac{q^3}{8\pi h\phi} \quad \text{and} \quad B_{FN} = -\frac{4\pi(\phi)^{1.5}\sqrt{8m}}{3qh}$$

Where F is the electric filed across the oxide, ϕ is the work function difference between two sides of the tunneling barrier, m is the electron effective mass in oxide. Noted that J_{FN} is exponentially proportional to the work function ϕ at power of 1.5.

Fowler-Nordheim tunneling usually exists on thin oxide with thickness larger than 5 nm. When the silicon oxide thickness goes below 4 nm, the tunneling process is dominanated by so called direct tunneling, which occurs through a trapezoidal barrier under relative lower external applied voltage. The direct tunneling current density is

$$J_T = \frac{2q}{h(2\pi)^2}\int_0^{\infty} \Delta f \left(\iint P dk_y dk_z\right) dE$$

Where P is the tunneling probability, Δf is the probability difference of states being occupied in and outside the barrier, k is the wave vector in plane of barrier. After approximation we have:

$$\mathrm{J}_T = \mathrm{A}_T \mathrm{F}^2 exp\left(-\frac{B_T}{F}\right)$$

$$\mathrm{A}_T = \frac{q^3}{8\pi h\phi}\frac{1}{\left(1-\sqrt{1-\frac{qV_{ox}}{\phi}}\right)^2} = \mathrm{A}_{FN}\frac{1}{\left(1-\sqrt{1-\frac{qV_{ox}}{\phi}}\right)^2}$$

$$B_T = -\frac{4\pi(\phi)^{1.5}\sqrt{8m}}{3qh}\left[1-\left(1-\frac{qV_{ox}}{\phi}\right)^{1.5}\right] = B_{FN}\left[1-\left(1-\frac{qV_{ox}}{\phi}\right)^{1.5}\right]$$

where V_{ox} is the voltage across the oxide layer. However even after approximation the result can express direct tunneling current with applied voltage analytically [24].

In ballistic transport no scattering is involved. This implies that the transport medium is either vacuum or a channel whose length shorter than the mean free path:

$$\langle x\rangle = \frac{k_B T}{\sqrt{2}\pi d^2 P}$$

The mean free path in air ambient is around 65 nm. The carrier transport in highly insulating medium (such as in vacuum) is governed by the space-charge-limited effect, and the resulting current density is determined by the Langmuir-Child's Law:

$$J_{LC} = A_{LC} V^{1.5}$$

$$A_{LC} = \frac{4\varepsilon_0}{9d^2}\sqrt{\frac{2q}{m_e}}$$

where q is the electron charge, d is the distance of transport. J_{LC} has the power-dependence of 1.5 to the applied voltage V [25].

When electron emission and transport in bulk solid such as semiconductor or insulator, the Langmuir-Child's Law needs to be revised taking into account the collision between electrons and thermal vibration, chemical impurities and lattice defects. Mott-Gurney's equation, another form of space-charge-limited current, gives the relationship between applied voltage V and current density J_{MG} in this case:

$$J_{MG} = A_{MG} V^2$$

$$A_{MG} = \frac{9\varepsilon_s \mu}{8d^2}$$

where ε_s is the dielectric constant of the transport media, μ is the mobility of electrons in this media and d is the distance of transport. As we saw, the power-dependence between J and V increased to 2.

4.2 TWO TERMINCAL I-V CHARACTERIZATION SYSTEM SET UP

A tungsten probe with tip diameter of 10 μm was used as top gate electrode in applying voltage bias. Sample was mounted on copper plate with thin gallium in between. Two terminal current-versus-voltage (I-V) characterizations were carried out with semiconductor parameter analyzer HP4145B (Figure 22).

In our experiments, silicon dioxide is designed to be less than 5 nm in order to make sure that a significant amount of tunneling can occur. Both dark and photo I-V characteristics were measured at the same probing point to understand the optoelectronic properties of GOS structures. The HP145B will scan from -2 V to +2 V with step of 0.01 V, recording the I-V data in the meanwhile.

The forward and reverse I-V results are plotted under two different forms to fully understand the working mechanism: linear-linear scale and log-log scale plots. The power law dependence $I \propto V^a$ (a is the slope in log-log scale and is in the range of 1.5-3.0) usually indicates the space-charge-limited current flow.

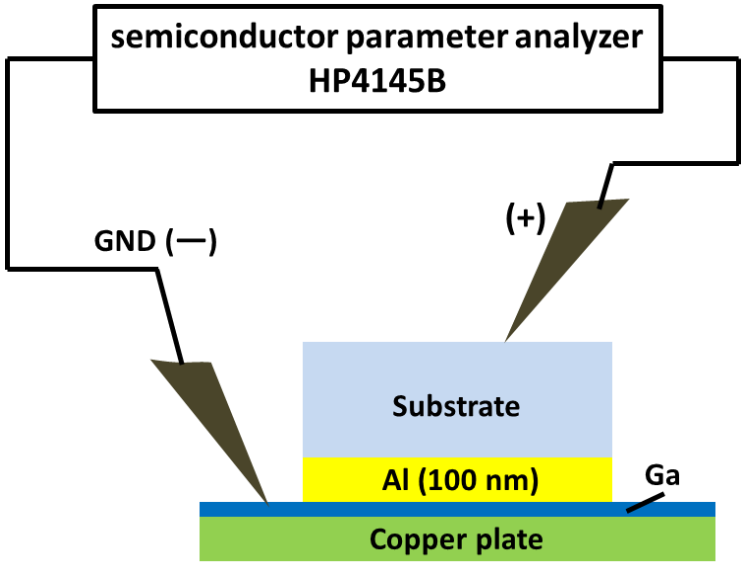


Figure 22 Two terminal I-V characterization system set up.

4.3 RESULTS AND DISCUSSION

4.3.1 I-V characteristics of GOS structure on p-Si

Two sets of samples were prepared to compare the tunneling effect in GOS structure with 2nm or 4nm thickness oxide. The size of silicon substrate is 2 cm x 2cm and the graphene electrode is 1.5 mm x 1.5 mm (Figure 23).

Reference samples were also prepared: same thickness oxide layer was grown on original silicon substrate, and the substrate experienced the same CMP process to understand the polishing (damage) effect.

Figure 24 shows the I-V characteristic of graphene/4 nm SiO_2/p-Si structure. When the sample is under forward bias (i.e., the graphene is negatively biased), the majority carriers accumulate on each side of the oxide layer and tunnel through the thin oxide. The tunneling current usually reveals a steeper rise than the usual power law. The I-V characteristic observed with this sample shows a power dependence of V^2. This indicates the overall carrier transport is limited by the space charge effect, not by the tunneling transport. The power law dependence observed with this sample is ascribed to the relatively low density of states available in graphene.

Under illumination at reverse bias, photo-generated electron-hole pairs are separated by the depletion field in the region under graphene. Electrons (and holes) travel to the interface and tunnel through the thin oxide, generating photocurrent. The photocurrent maintains a slope of 1 at low voltage and then rises/saturates at ~34 μA at higher voltage for 0.1 mW input power. The

photo responsivity is calculated to be 0.34 A/W and external quantum efficiency (EQE) is 66%. The same structure with thinner oxide (2 nm) reveals a similar performance (Figure 25).

The I-V characteristic after CMP is shown at Figure 26 and Figure 27. Under forward bias, the dark current rises slowly, first showing $I \propto V^{1.5}$ and then increases to a power dependence of $I \propto V^2$ after – 0.4 V. Under reverse bias, the photocurrent increases sharply after a slope of ~1 at lower voltage. The photo responsivity for 2 nm and 4 nm case is measured to be 0.28 A/W and 0.33 A/W respectively. After chemical-mechanical polishing (CMP) process, the I-V characteristic (dark and photo) remains similar to the sample without CMP.

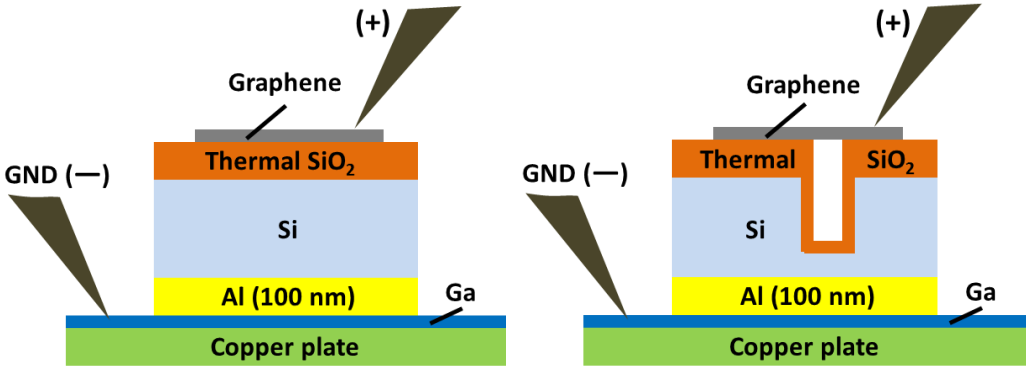


Figure 23 GOS structure with and without nano-channels and probing set up

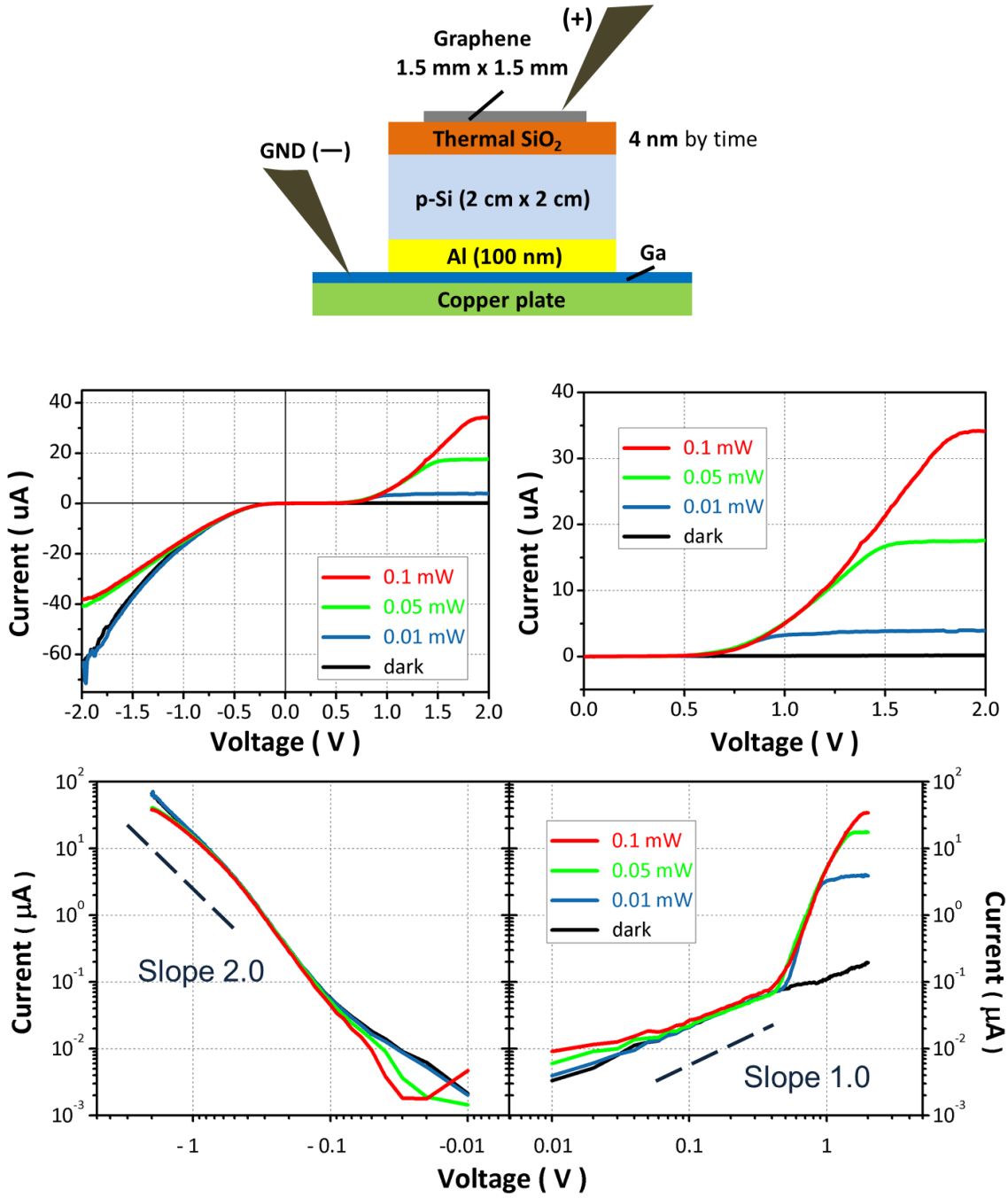


Figure 24 I-V characteristic of graphene/4 nm SiO_2/p-Si sample in linear-linear scale (top) and log-log scale (bottom) plot.

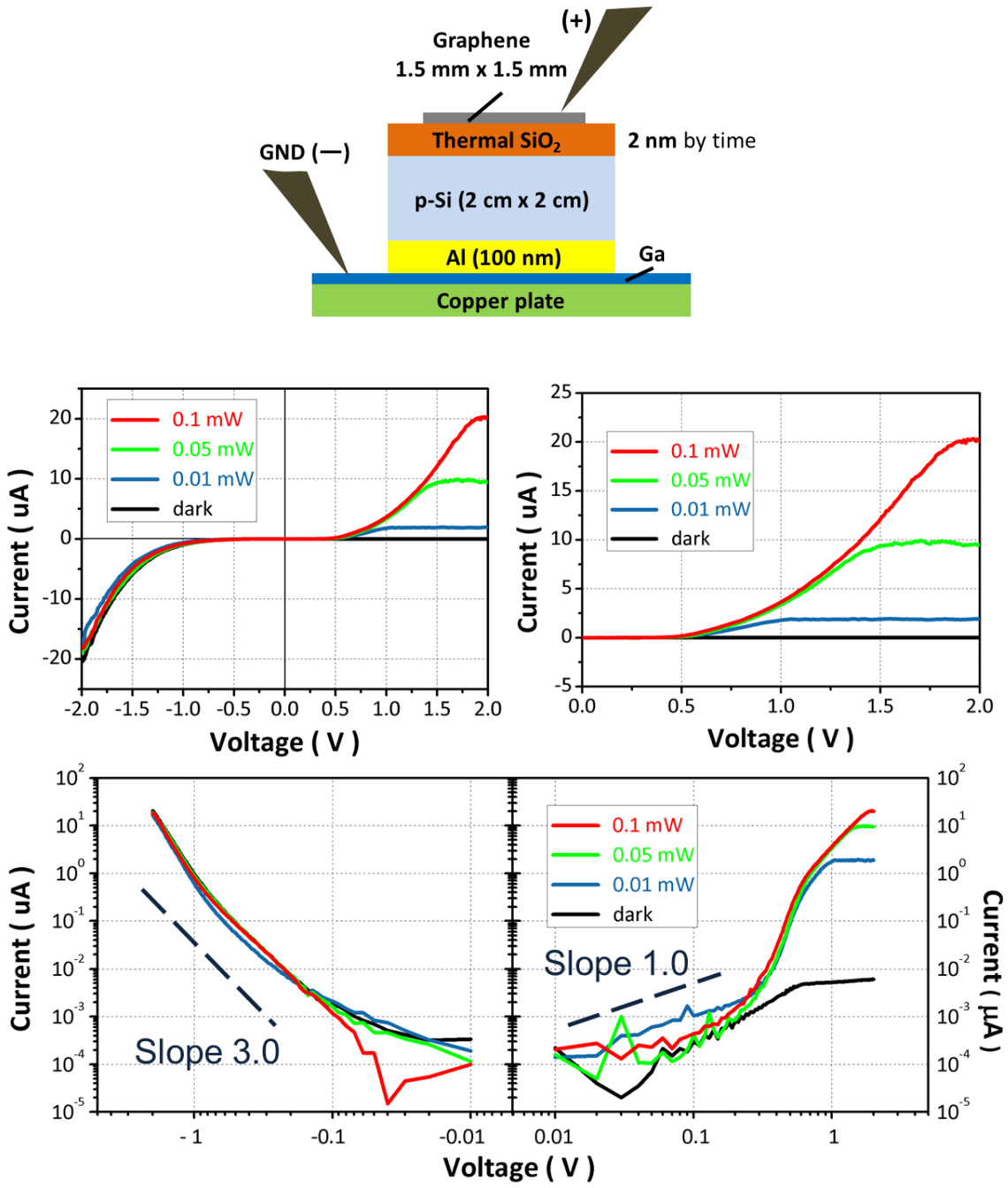


Figure 25 I-V characteristic of graphene/2 nm SiO_2/p-Si sample in linear-linear scale (top) and log-log scale (bottom) plot.

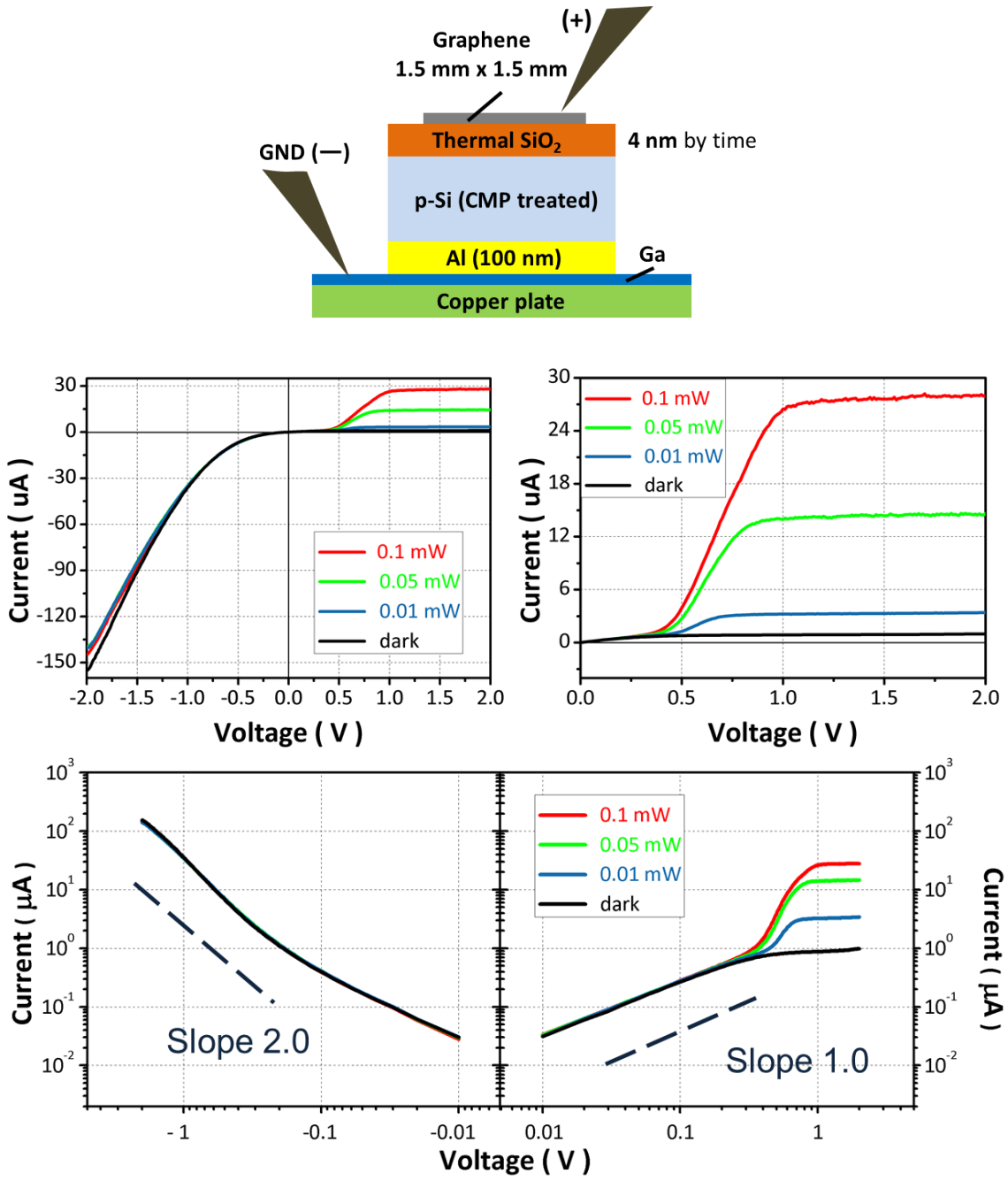


Figure 26 I-V characteristic of graphene/4 nm SiO_2/p-Si after CMP treatment in linear-linear scale (top) and log-log scale (bottom) plot.

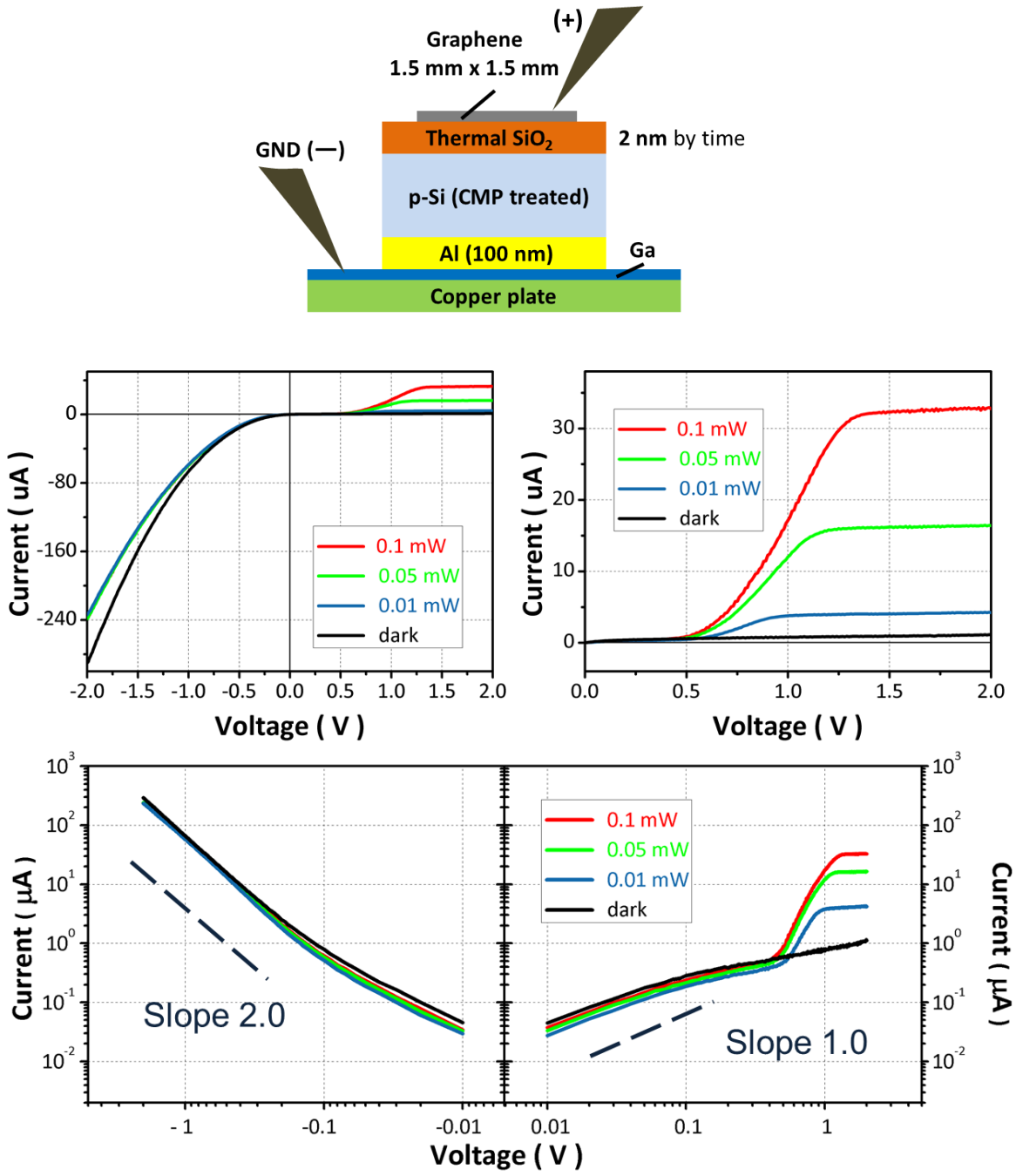


Figure 27 I-V characteristic of graphene/2 nm SiO_2/p-Si after CMP treatment in linear-linear scale (top) and log-log scale (bottom) plot.

4.3.2 I-V characteristic of GOS structure with nano-channels on p-Si

Introducing nano-channels to the GOS structure results in two different regimes of slope in forward bias (Figure 28, Figure 29 and Figure 30). The dark tunneling current gives $I \propto V^1$ dependence below 1 V and $I \propto V^2$ at higher voltage. With a thick (22 nm) oxide (Figure 30) the dark current gives $I \propto V^{1.5}$ dependence below 1 V and $I \propto V^2$ at higher voltage. This suggests another transport mechanism is induced by the nano-channels. The nano-void-channels provide a transport medium for kinetic electrons to ballistically travel. Electron will accumulate under forward bias (graphene positively biased) at the interface forming a two-dimensional electron gas (2DEG) layer. The Coulombic repulsion between electrons in 2DEG will push the electrons on the edge to emit into air. Top electrode captures the emitted electrons that transported through a void channel whose channel length (oxide thickness) is smaller than the mean free path of electrons in air. The phenomenon is similar to the electron transport mechanism in vacuum channels model and can be explained by the Langmuir-Child's law with power dependence of $V^{1.5}$. With an increase of applied voltage, collision becomes no longer negligible, and the space charge limited current will then be described by the Mott-Gurney's law with power dependence of V^2.

With 22nm-oxide samples (Figure 30) under reverse bias, the photo current saturates at ~33 μA for 0.1 mW input power. The sample has a photo responsivity of 0.33 A/W and 65 % external quantum efficiency (EQE).

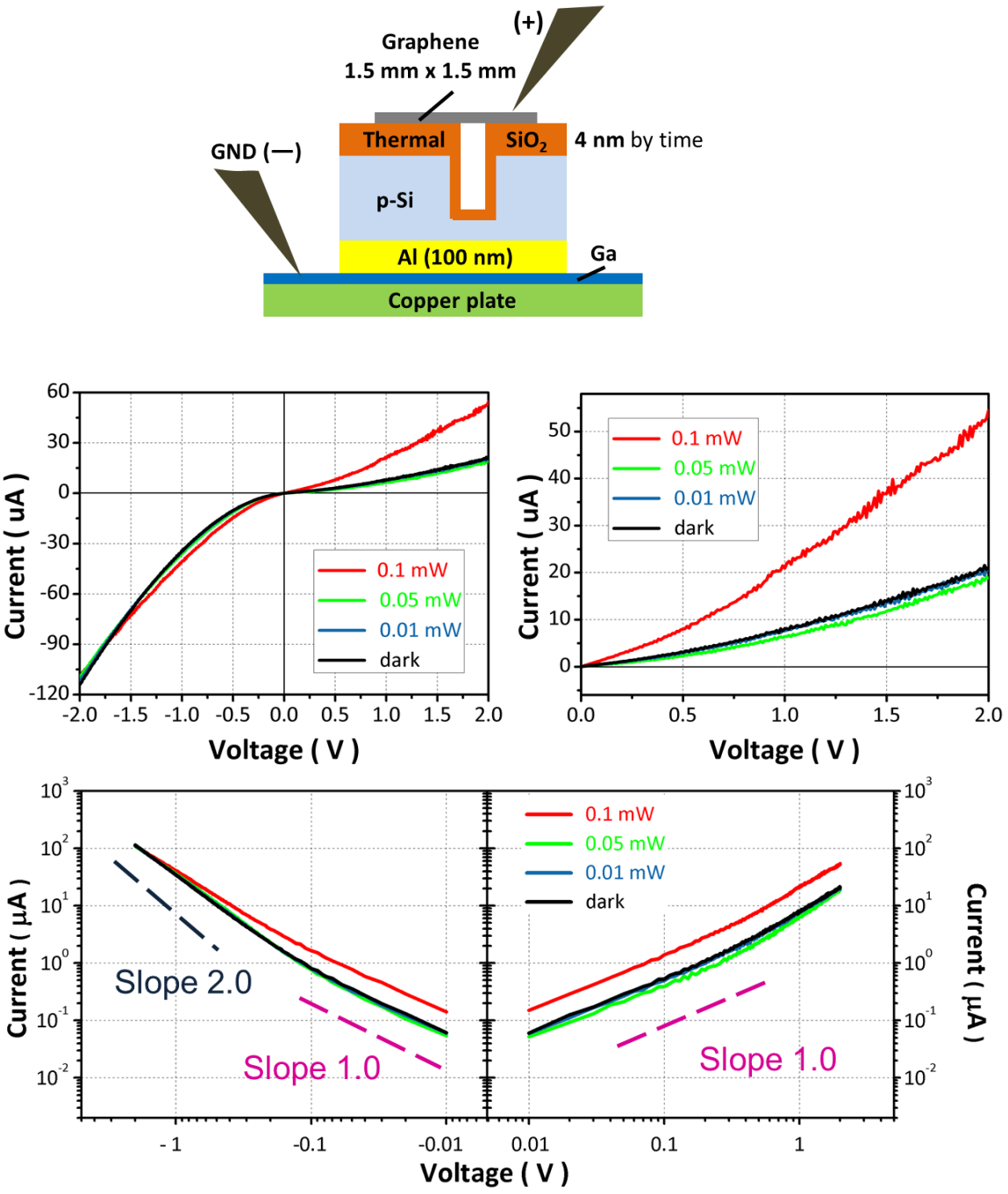


Figure 28 I-V characteristic of graphene/4 nm SiO_2/p-Si after CMP treatment with nano-channels in linear-linear scale (top) and log-log scale (bottom) plot.

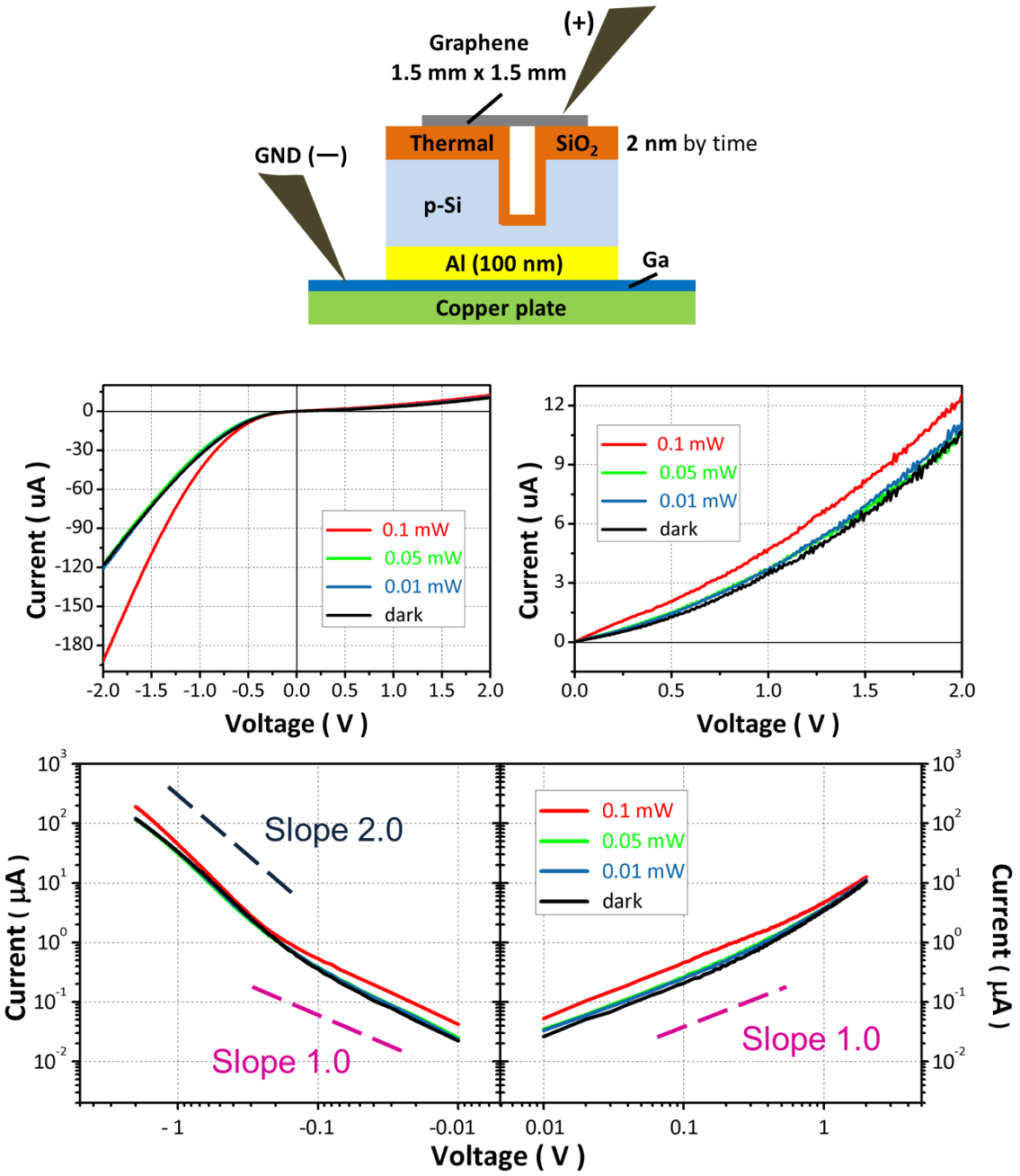


Figure 29 I-V characteristic of graphene/4 nm SiO_2/p-Si after CMP treatment with nano-channels in linear-linear scale (top) and log-log scale (bottom) plot.

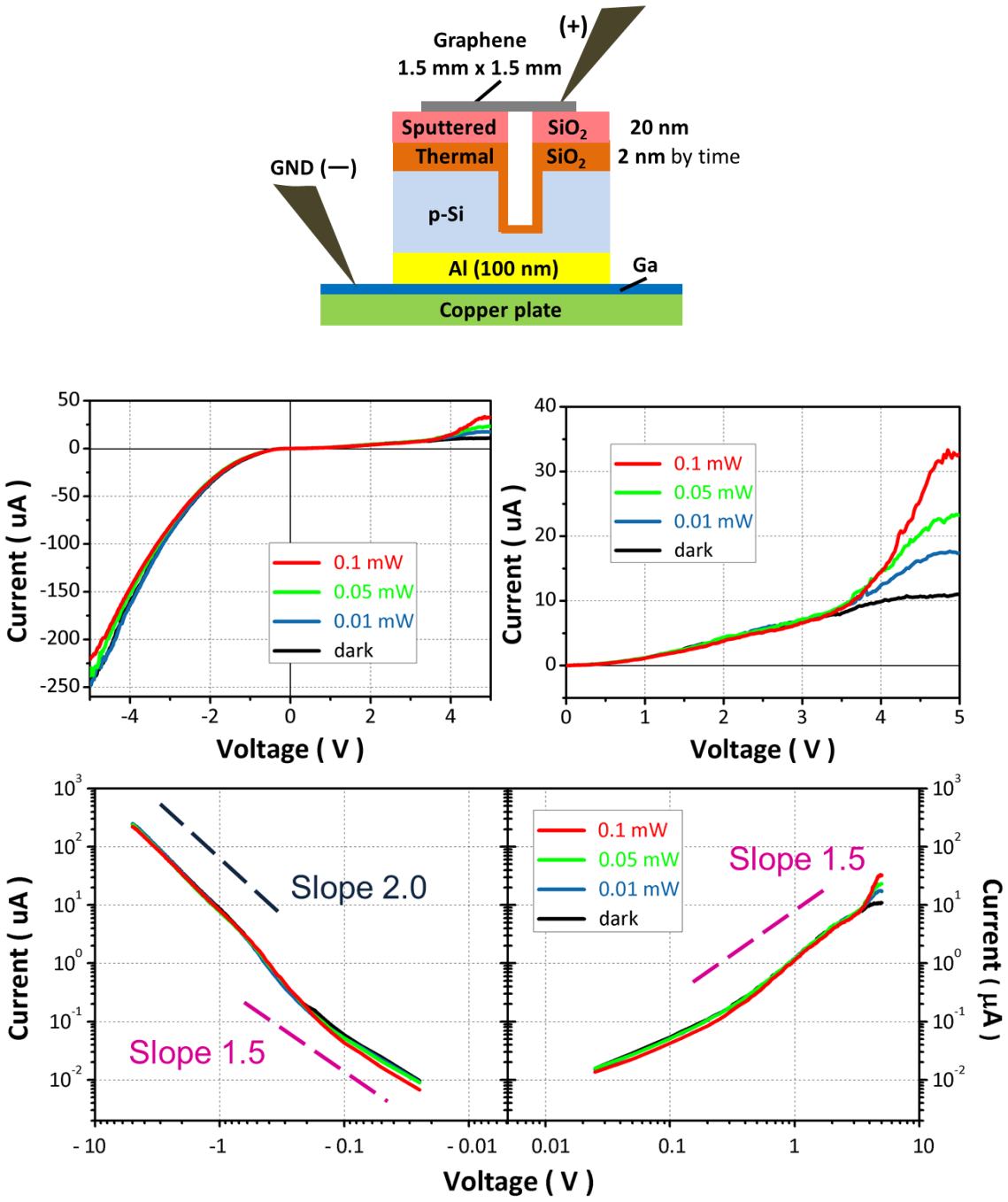


Figure 30 I-V characteristic of graphene/22 nm SiO_2/p-Si with nano-channels in linear-linear scale (top) and log-log scale (bottom) plot.

4.3.3 I-V characteristics of GOS structure on n-Si

Figure 31 shows the I-V characteristic of graphene/4 nm SiO_2/n-Si structure. When the sample is under forward bias, i.e., graphene is positively biased, electrons (holes) are attracted toward oxide interface and then tunnel through the thin oxide. The I-V characteristic reveals a power dependence of V^3 after 0.1 V. This power law indicates the carrier transport is still governed by the space charge effect, similar to the p-Si case. The slope of 3 suggests involvement of bipolar charge carriers (electrons and holes). The reverse saturation current is around 32 μA for 0.1 mW input power. The photo responsivity is 0.32 A/W and external quantum efficiency (EQE) is 63 % which is similar to p-type structure. The same structure with thinner oxide (2 nm) reveals similar slope (Figure 32). Compared to the thicker oxide, samples with 2nm oxide have less rectification and more leakage current. This suggests direct tunneling takes place when the oxide layer become ultrathin, increasing the leakage current. The reverse saturation is around 41 μA for 0.1 mW input power, corresponding to 0.41 A/W responsivity and 80 % EQE.

The I-V characteristic after CMP is shown in Figure 33 and Figure 34. Under forward bias, the dark current rises slowly first showing $I \propto V^1$ and then increases to a power dependence of $I \propto V^3$ at 0.4 V. Under reverse bias, the photo current increases sharply and then maintains a slope less than 1 before saturation. After CMP process, the leakage current increased and the I-V curve becomes less rectifying. CMP process is very likely to have induced defects on Si surface, which is expected to affect charge trapping and band bending, altering the transport properties. Compared to the p-type case the n-Si structure is more significantly affected by the CMP process.

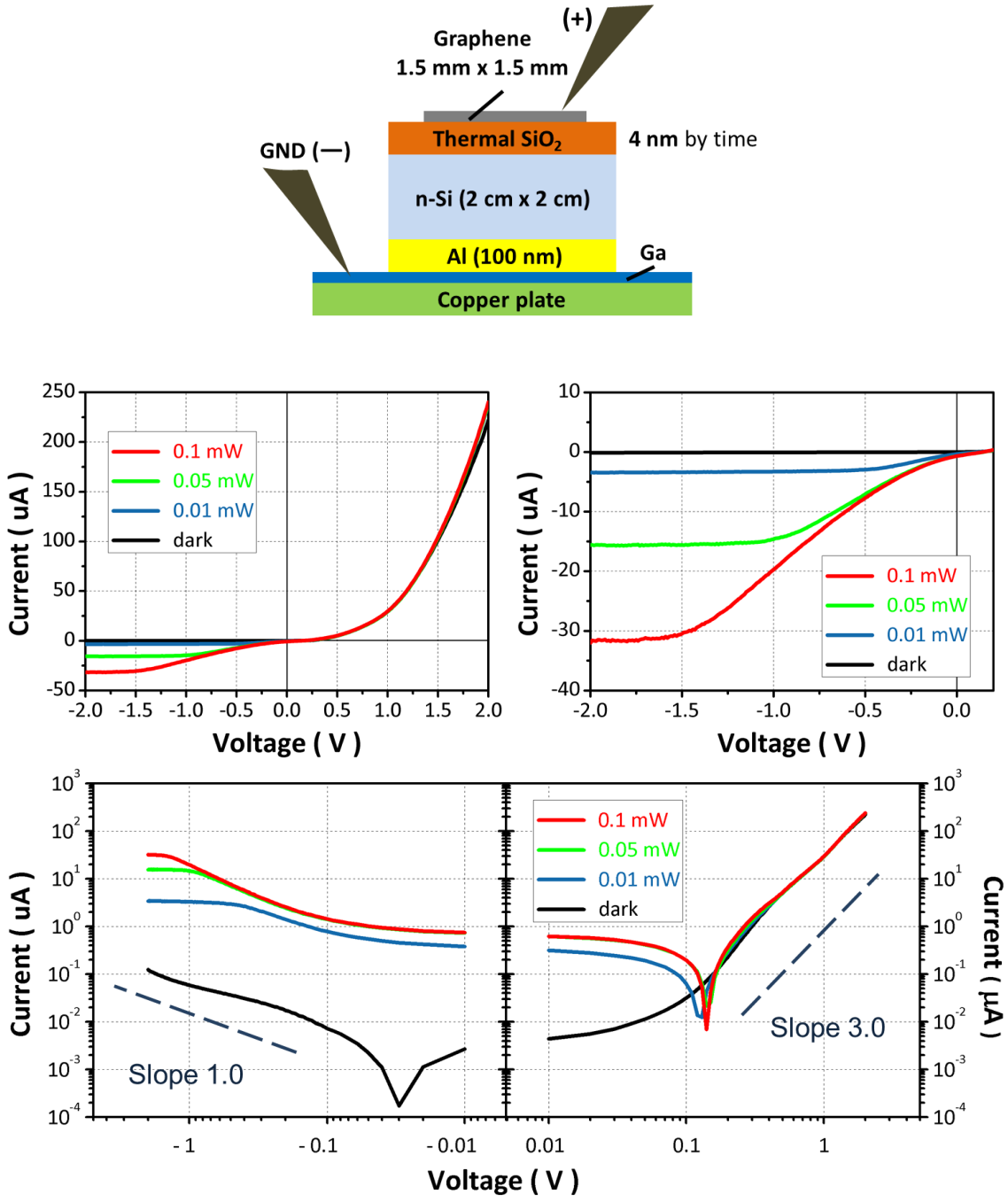


Figure 31 I-V characteristic of graphene/4 nm SiO_2/n-Si sample in linear-linear scale (top) and log-log scale (bottom) plot.

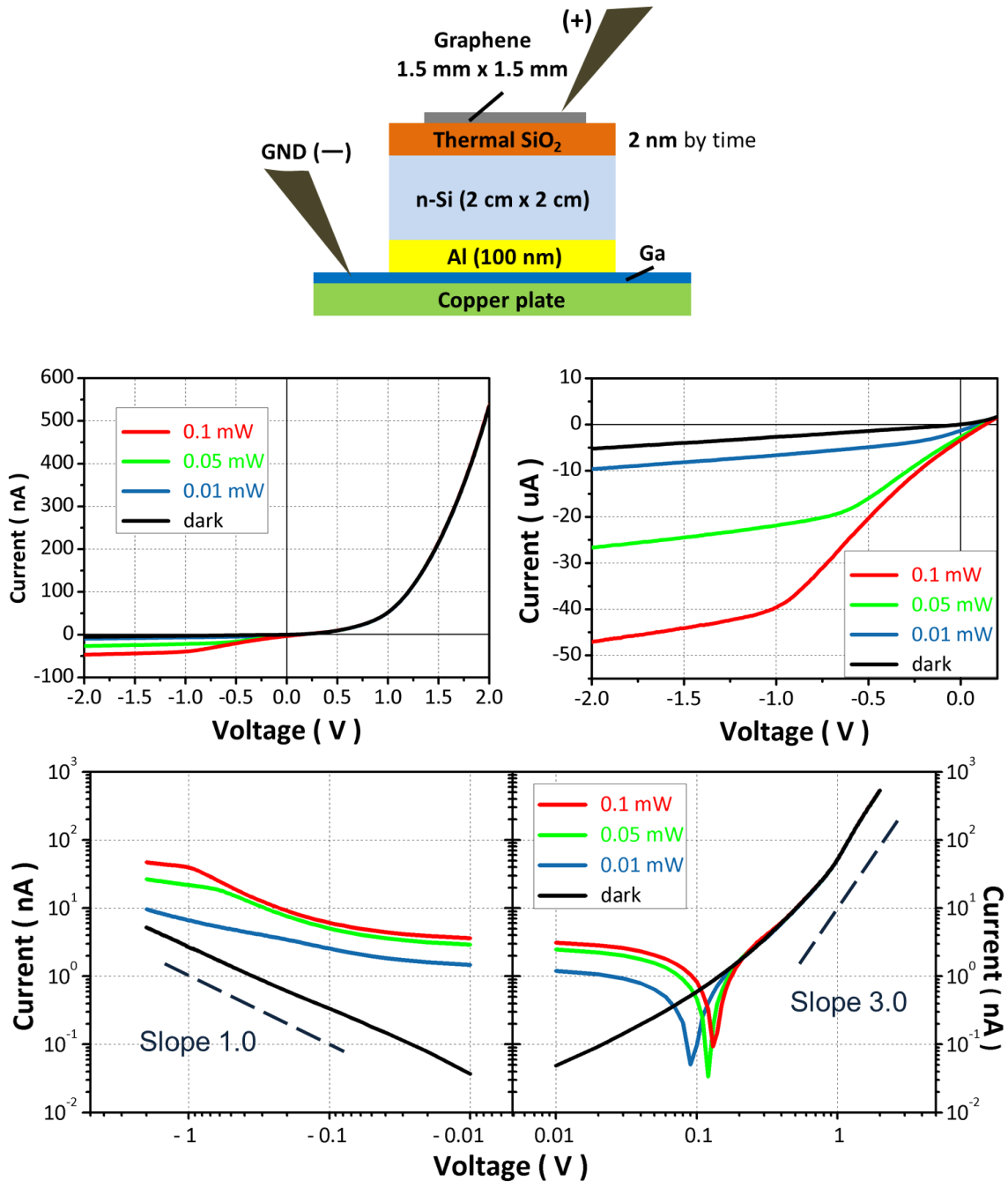


Figure 32 I-V characteristic of graphene/2 nm SiO_2/n-Si sample in linear-linear scale (top) and log-log scale (bottom) plot.

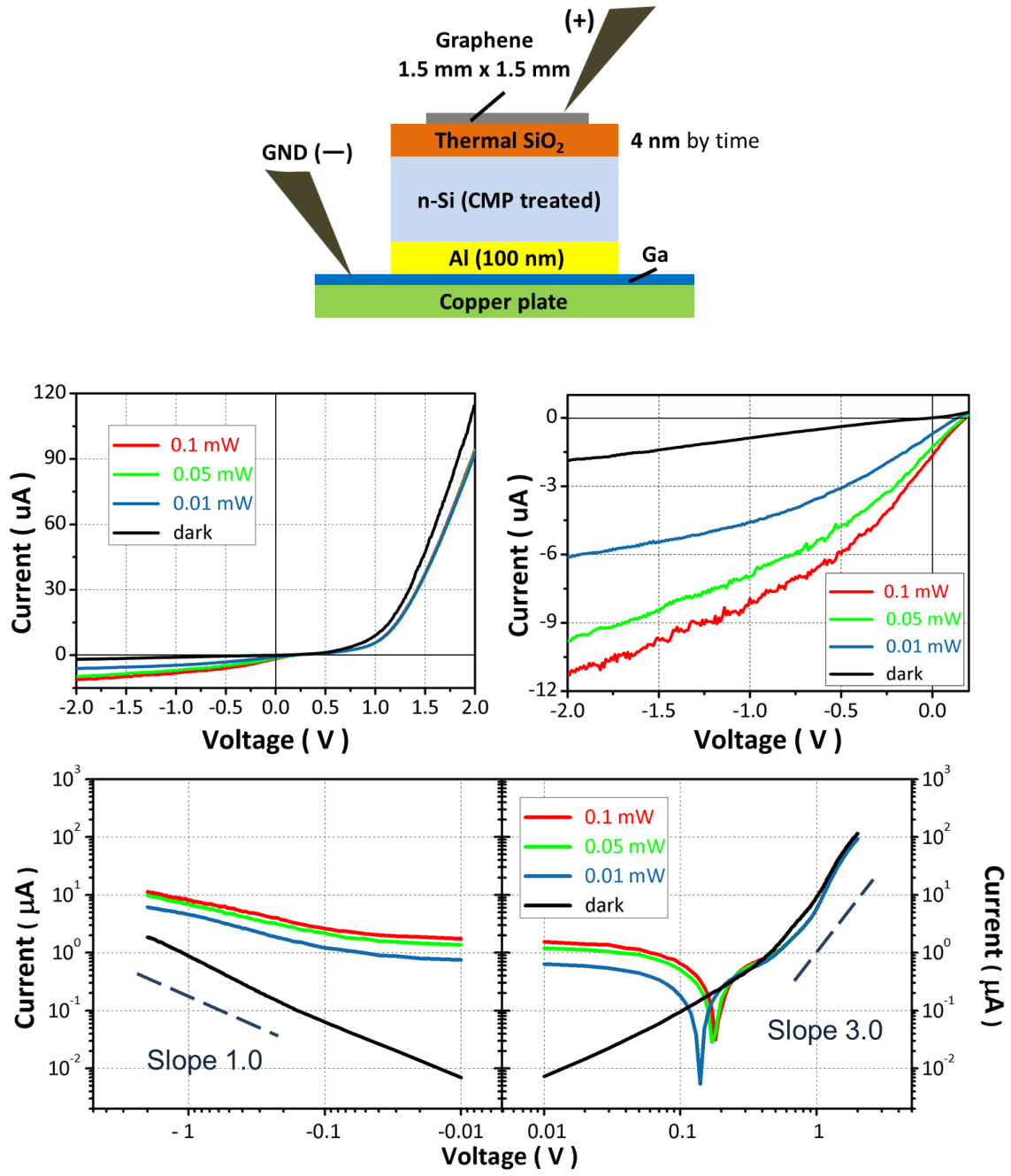


Figure 33 I-V characteristic of graphene/4 nm SiO_2/n-Si after CMP treatment in linear-linear scale (top) and log-log scale (bottom) plot.

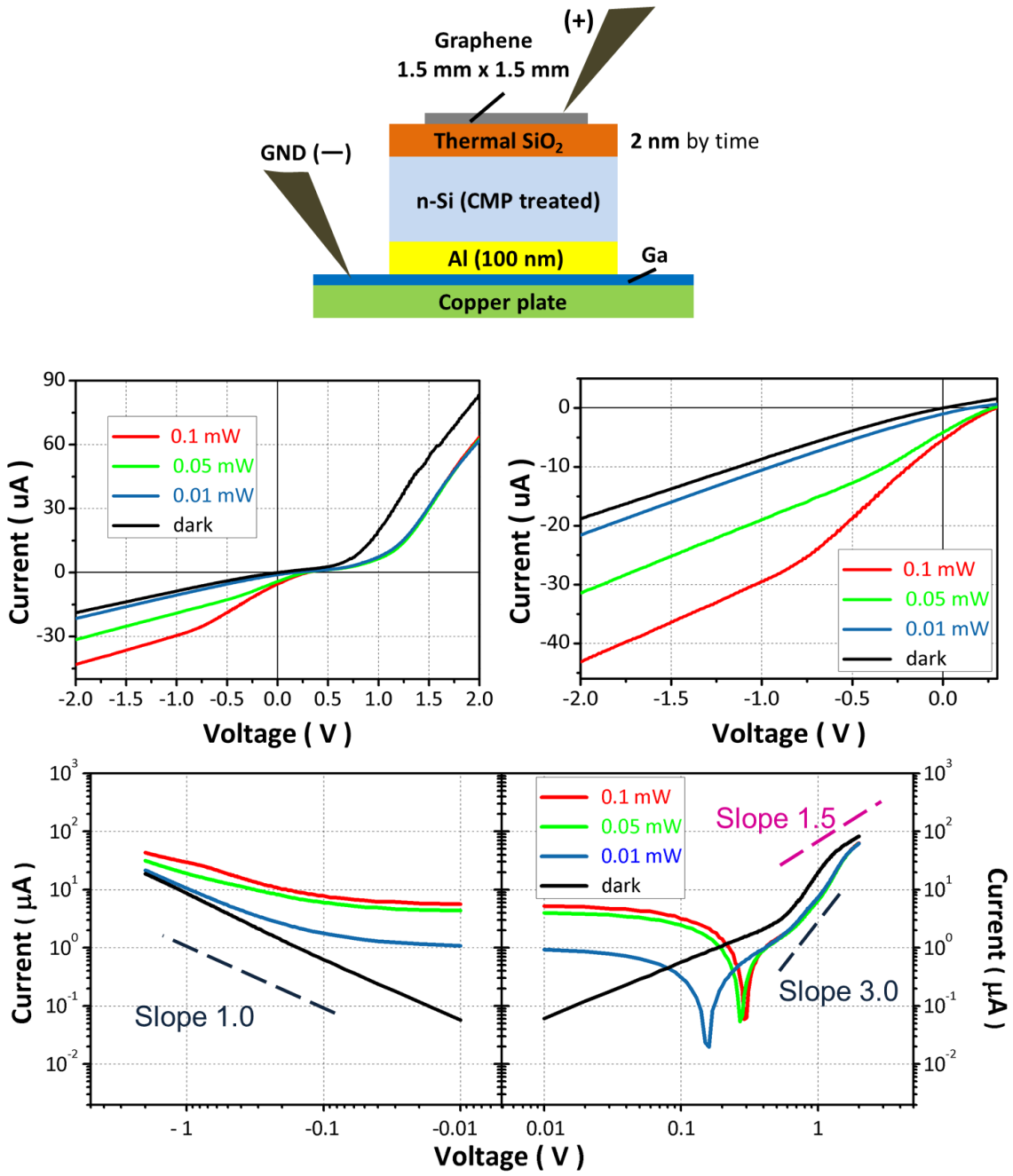


Figure 34 I-V characteristic of graphene/2 nm SiO_2/n-Si after CMP treatment in linear-linear scale (top) and log-log scale (bottom) plot.

4.3.4 I-V characteristics of GOS structure with nano-channels on n-Si

Introducing nano-channels results in a significantly larger slope in forward bias region (Figure 35). The dark tunneling current gives $I \propto V^{1.5}$ dependence below 1 V and $I \propto V^{5}$ at higher voltage. For 2 nm oxide (Figure 36), the dark tunneling current gives $I \propto V^{1}$ dependence below 1 V and $I \propto V^{4}$ at higher voltage. Unlike the regular slope appear on p-type samples, the trapping states in n-type samples apparently cause the power dependence of $I \propto V^{4}$ even V^{5}.

With 4 nm samples (Figure 35) under reverse bias, the photo current saturates at ~26 μA for 0.1 mW input power. The sample has a photo responsivity of 0.26 A/W and 50.9 % external quantum efficiency (EQE). The 2 nm samples (Figure 36) didn't show saturation within a safe voltage range.

The photo I-V curve always has a zero current crossing point between 0.1 V and 0.2 V for n-type samples, which appears as a dip in the log-log scale plot. The open circuit voltage (V_{oc}) will increase as the input light power increases. CMP process doesn't shift the V_{oc} (0.19 V comparing to 0.15 V at 0.1 mW), while the sample with nano-channel has open circuit voltage of 0.36 V at 0.1 mW. None of the p-type sample shows open circuit voltage under illumination implying that there is no built-in field inside the GOS structure.

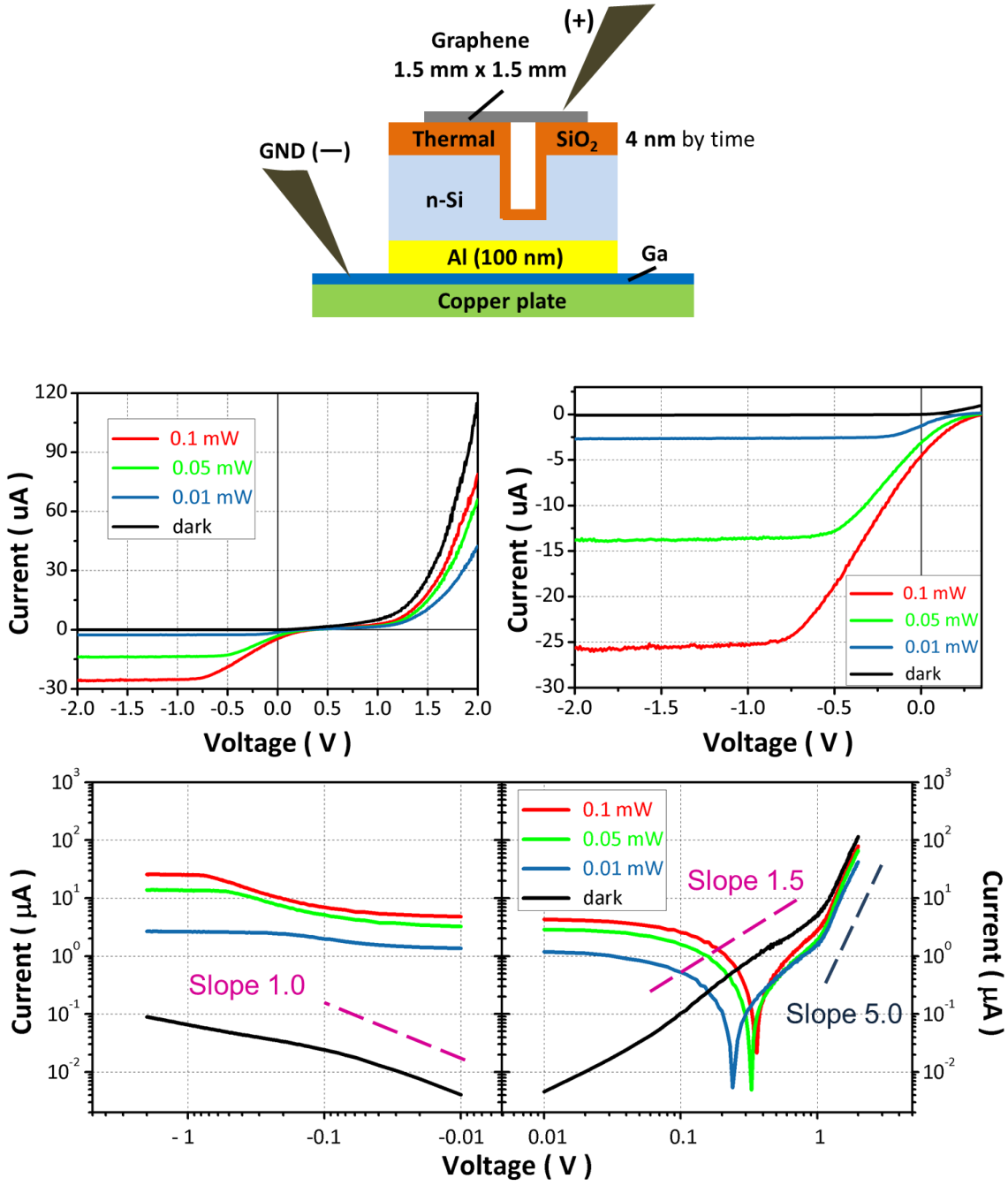


Figure 35 I-V characteristic of graphene/4 nm SiO_2/n-Si after CMP treatment with nano-channels in linear-linear scale (top) and log-log scale (bottom) plot.

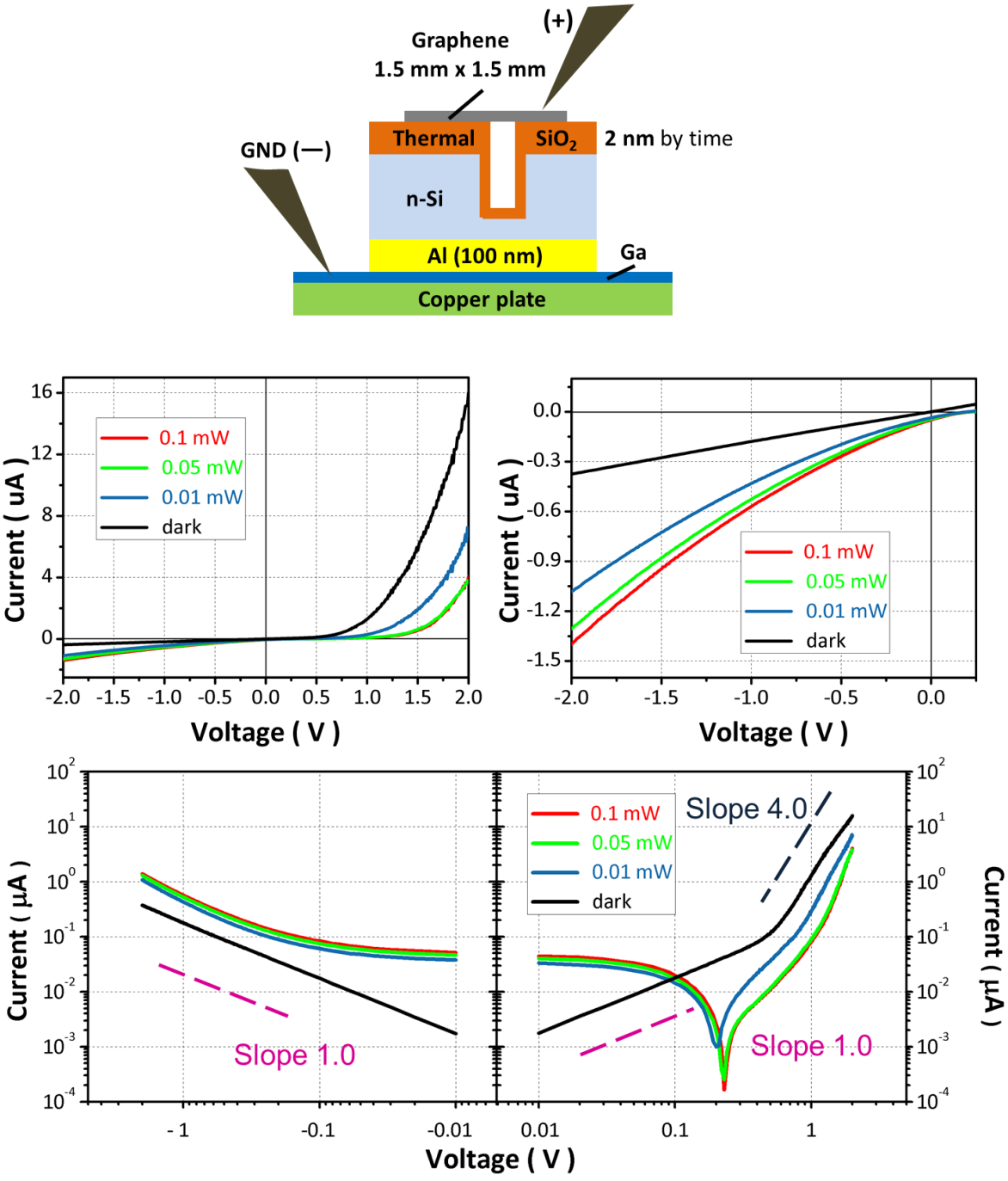


Figure 36 I-V characteristic of graphene/4 nm SiO_2/n-Si after CMP treatment with nano-channels in linear-linear scale (top) and log-log scale (bottom) plot.

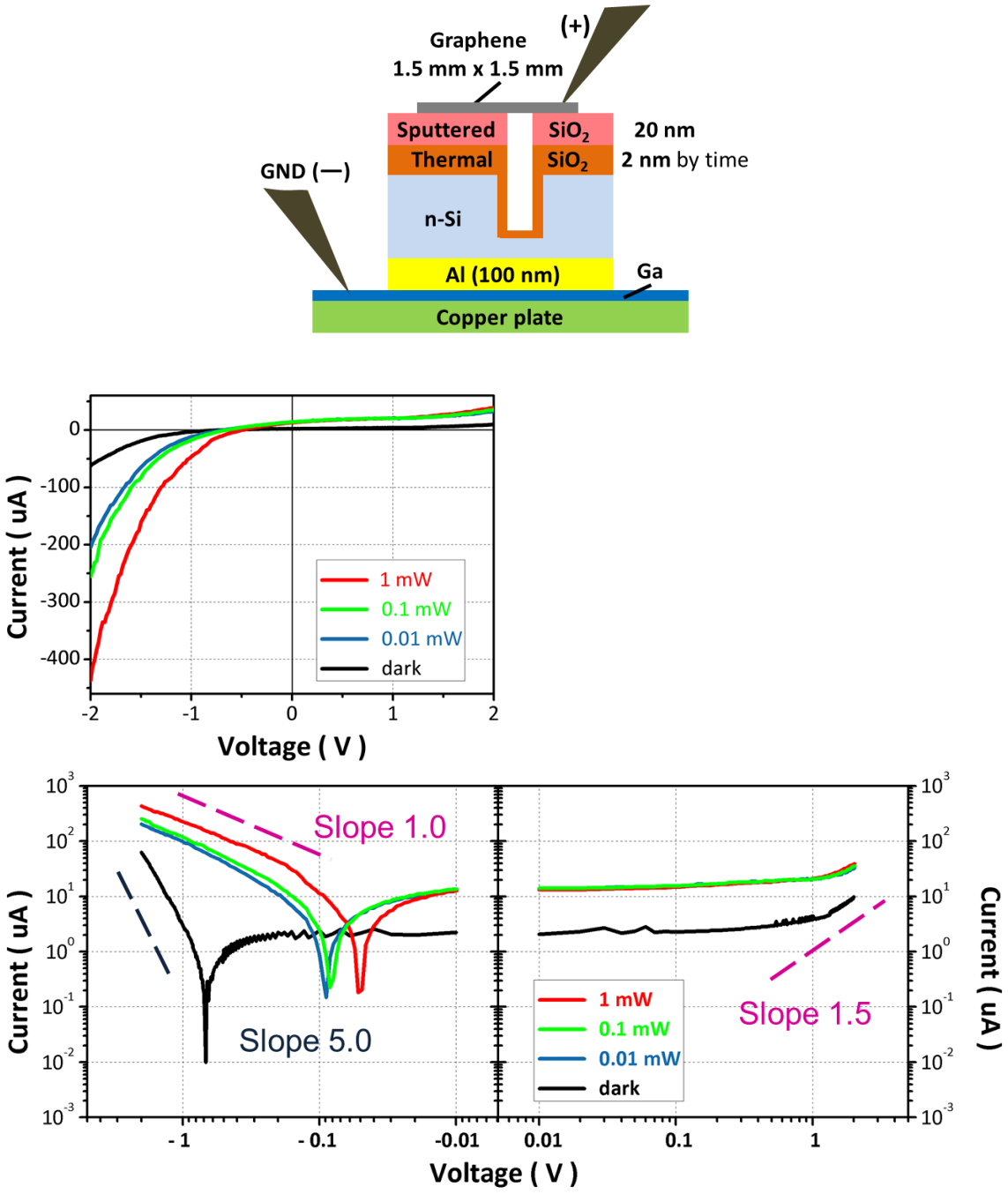


Figure 37 I-V characteristic of graphene/22 nm SiO_2/n-Si with nano-channels in linear-linear scale (top) and log-log scale (bottom) plot.

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